

FIG. 1

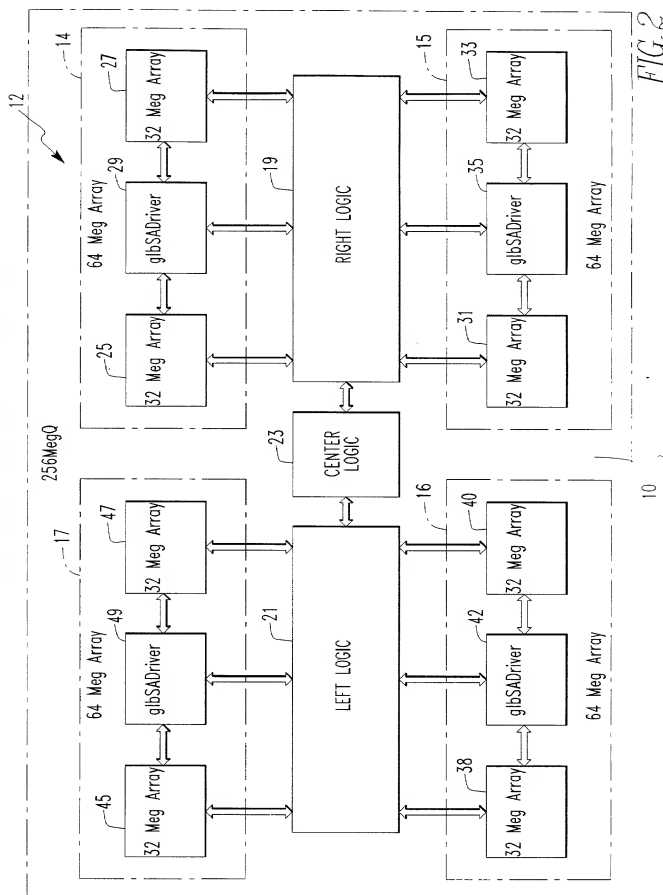
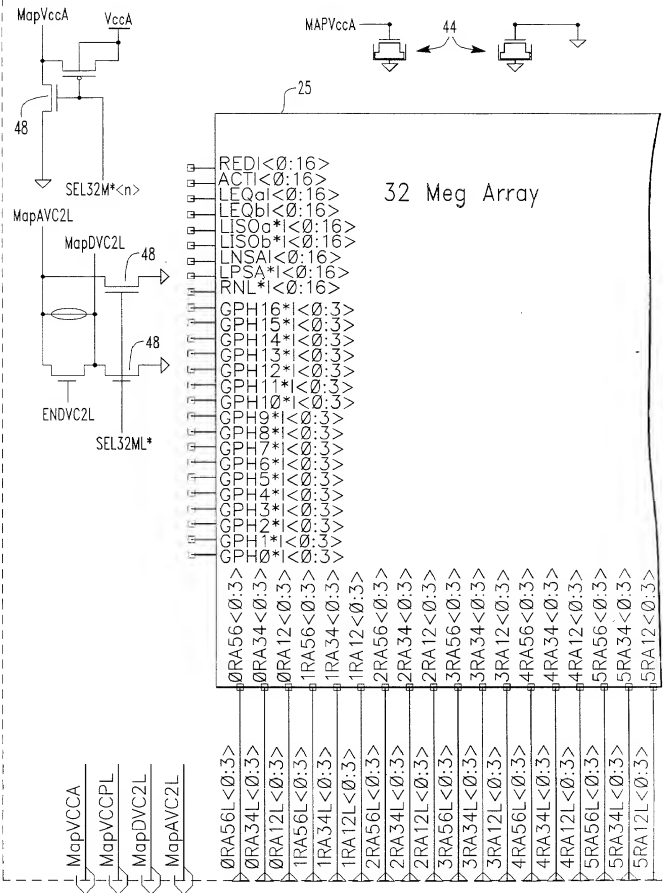
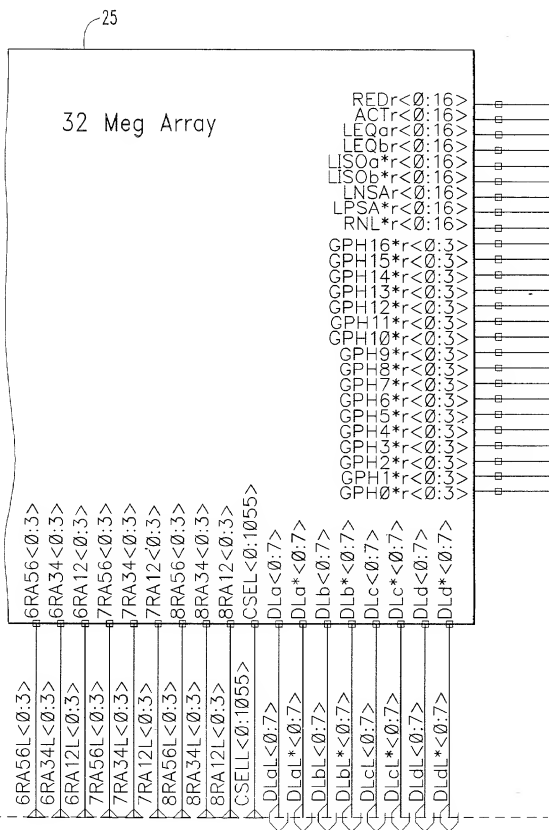


FIG. 3A





-29

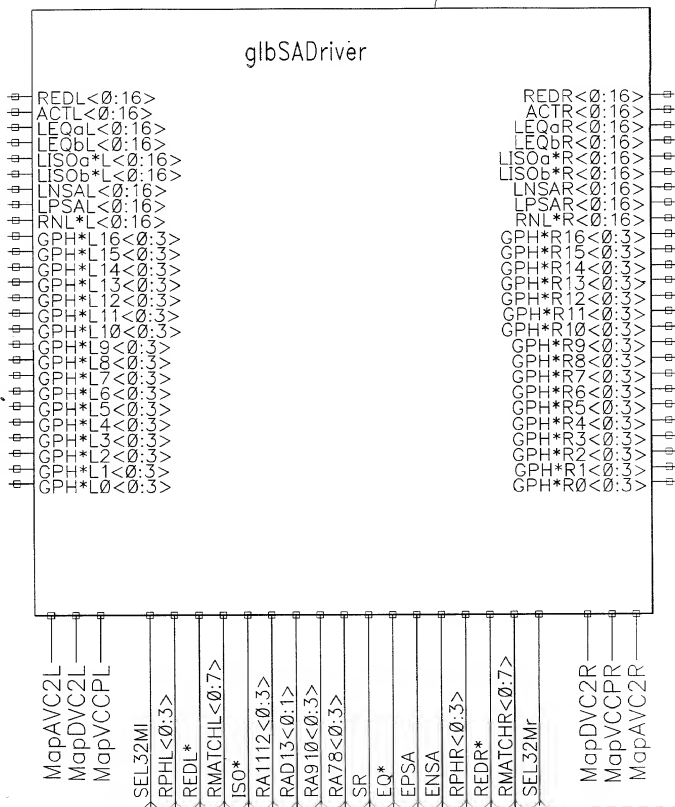
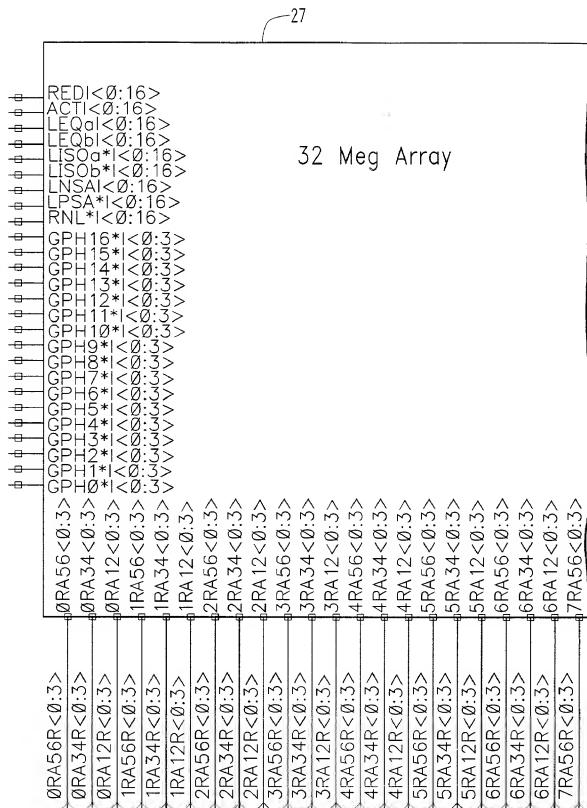


FIG. 3D



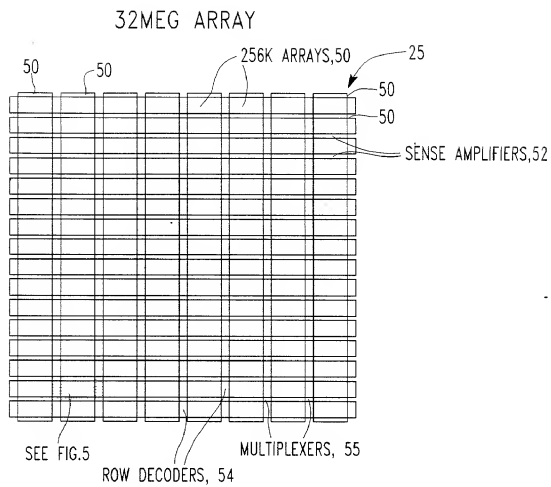


FIG. 4

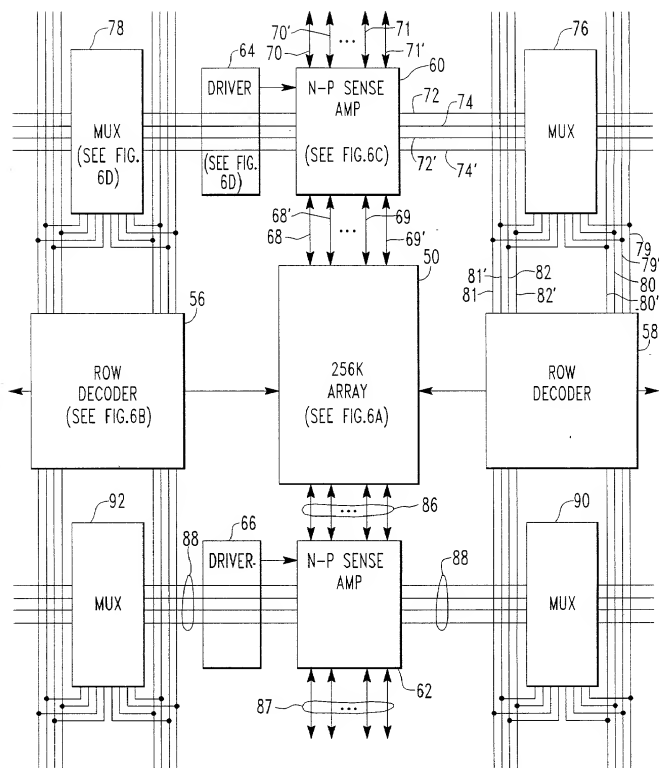


FIG. 5

10/367

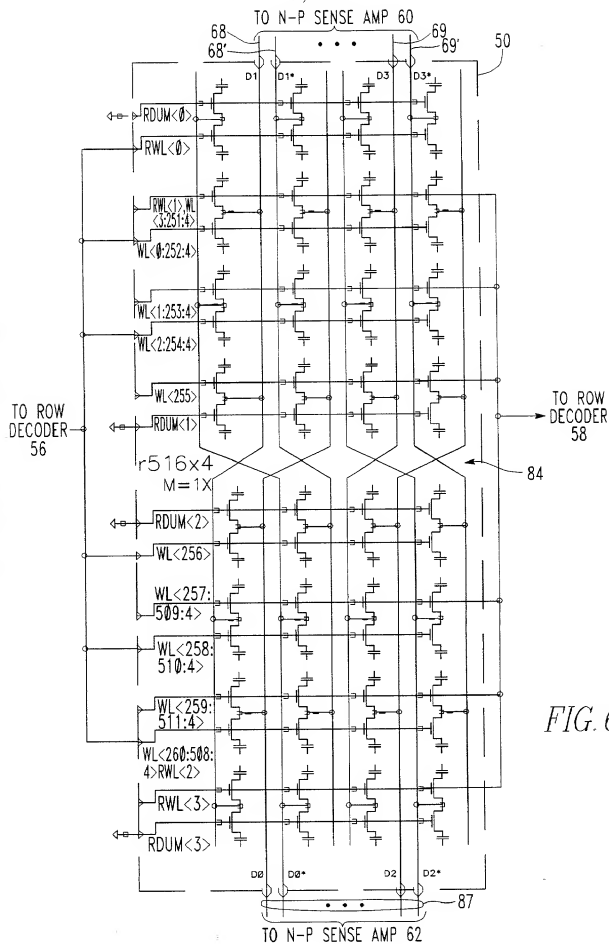
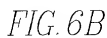


FIG. 6A



12/367

Connections of odd/even
columns to IOa and IOb
alternates with odd/even
column select lines:

CA01* D1(even) D2(odd)

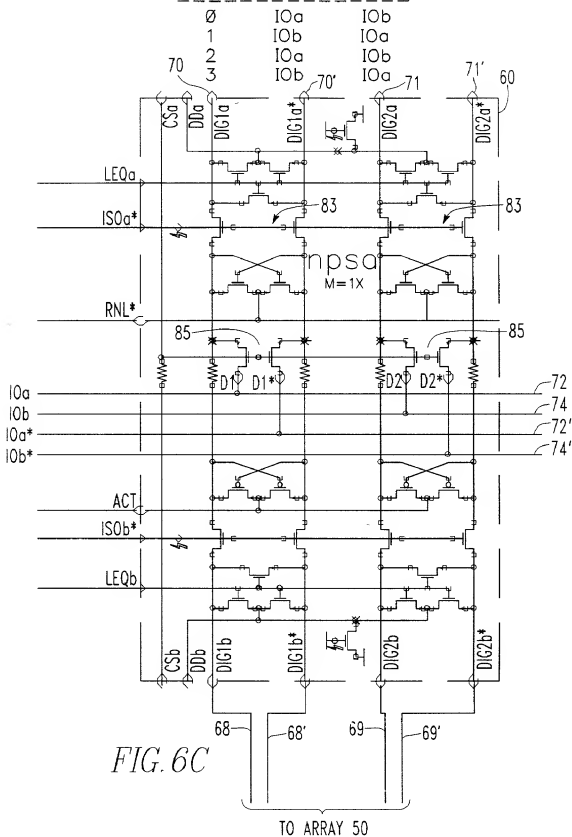


FIG. 6C

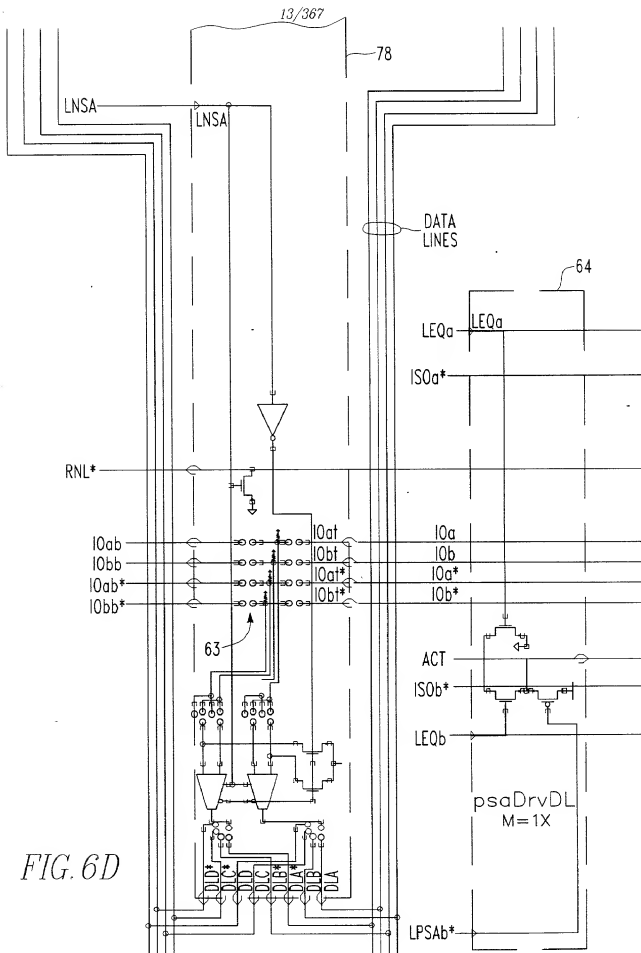


FIG. 6D

25

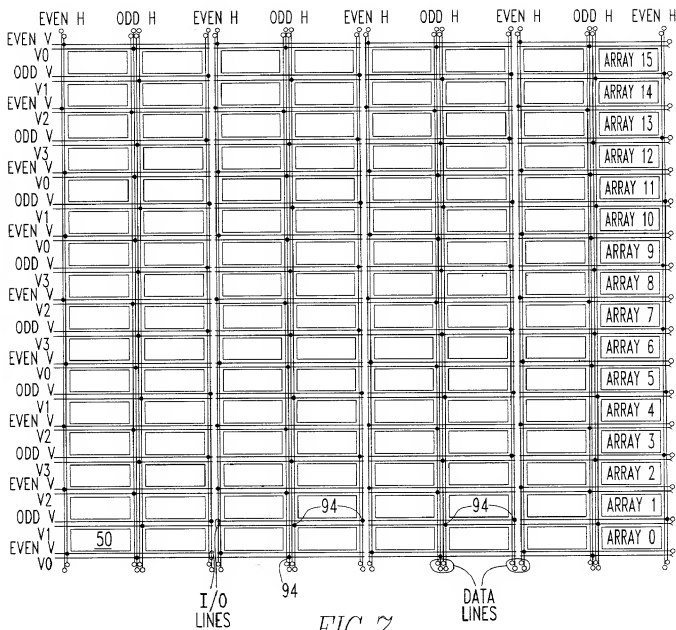


FIG. 7

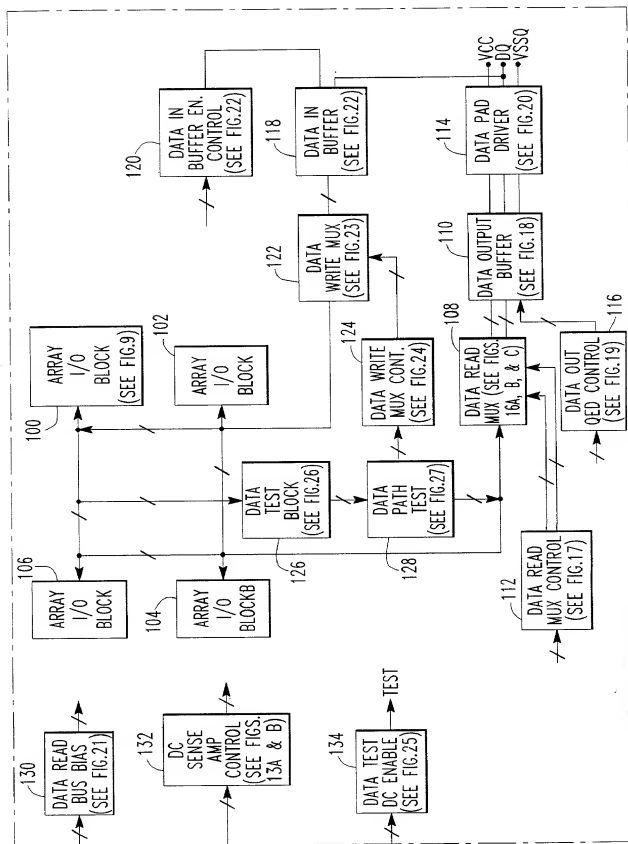


FIG. 8

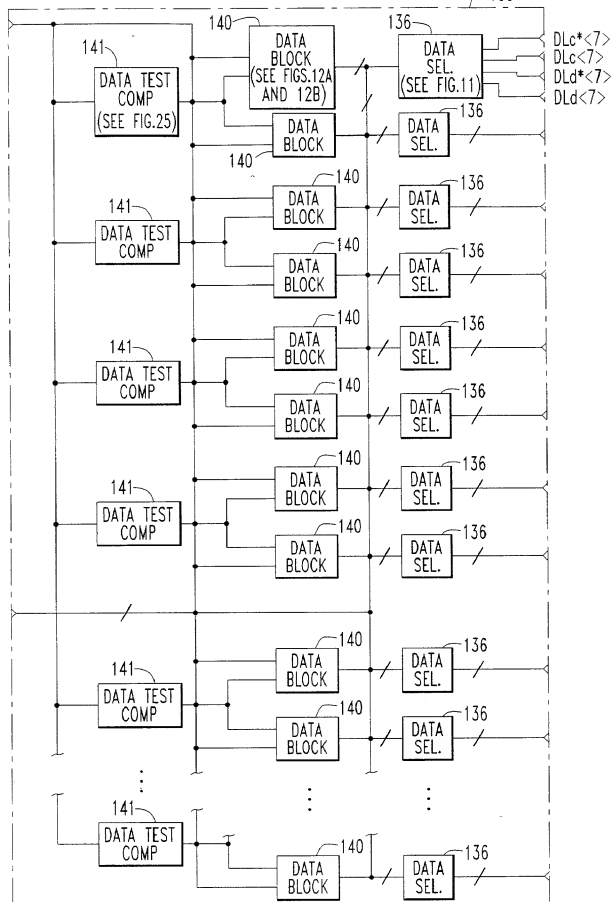
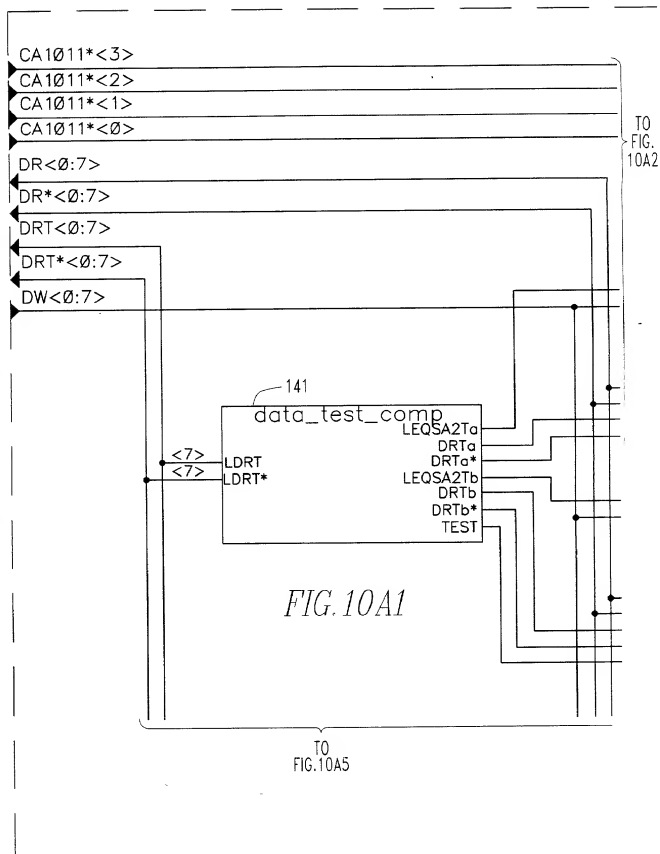


FIG. 9



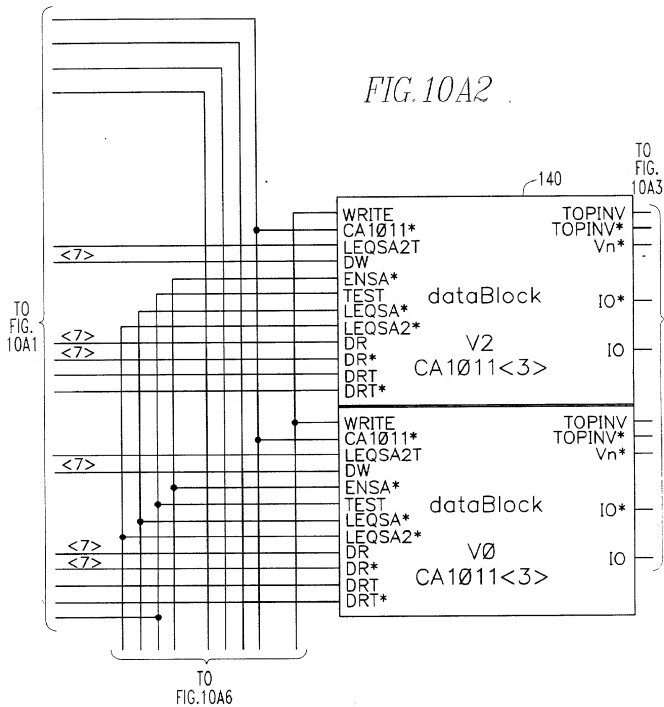
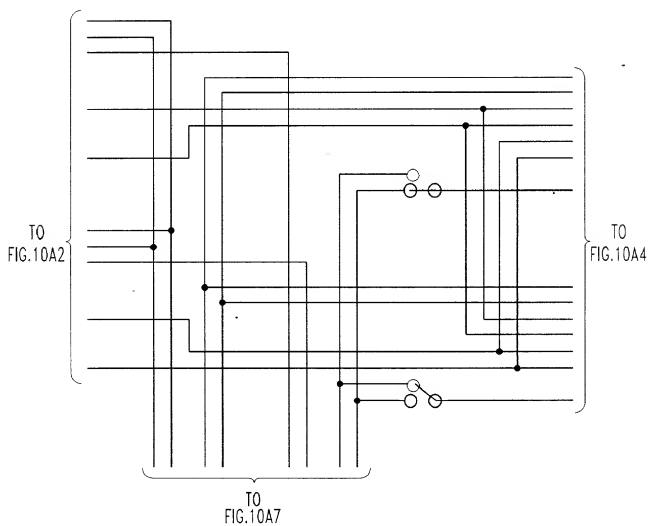


FIG. 10A3

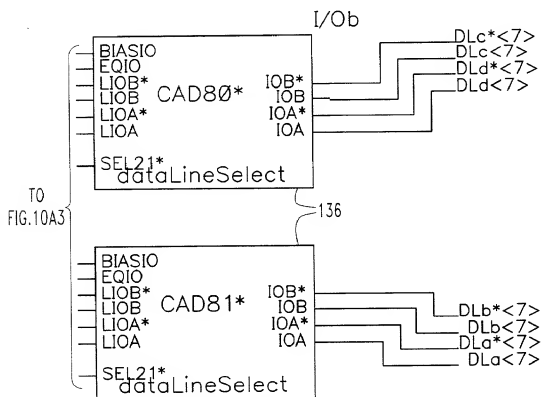


00004529.030001

arrayIOBlock

100

FIG. 10A4



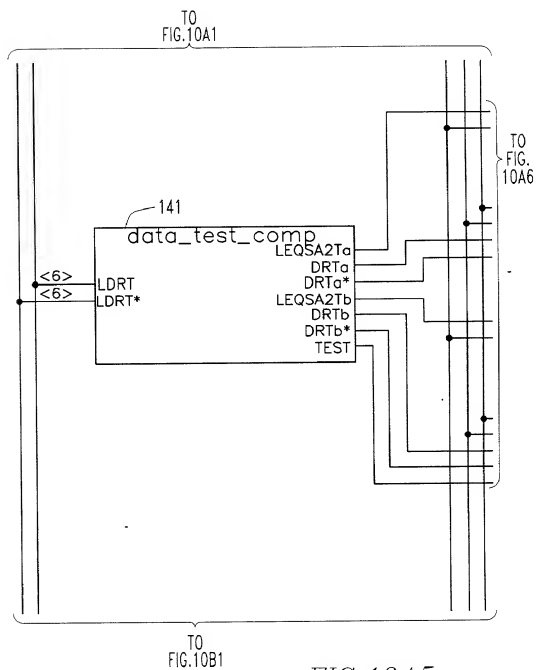


FIG. 10A5

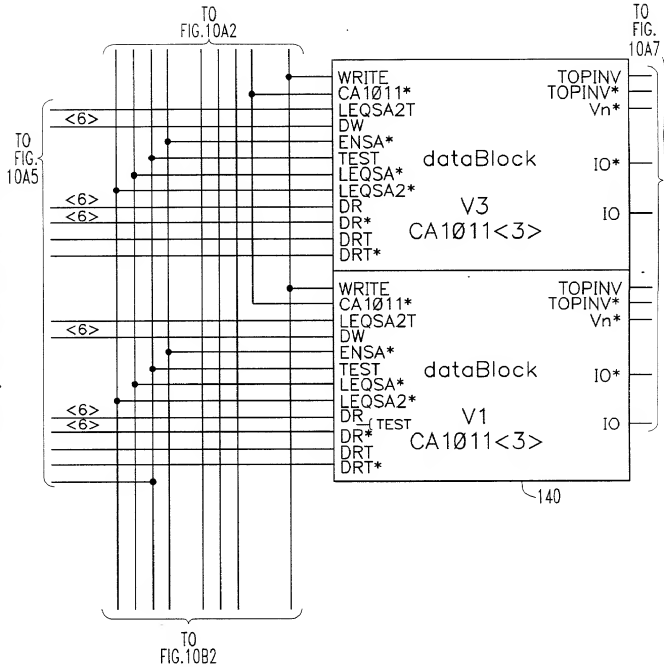


FIG. 10A6

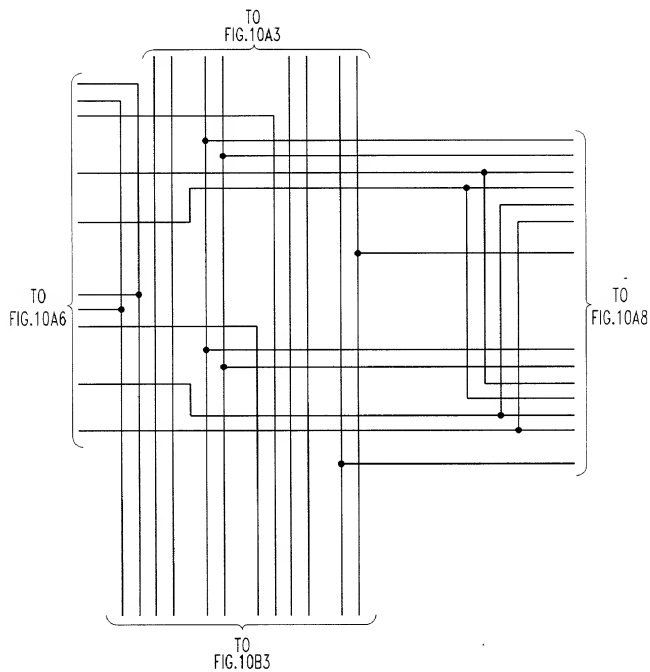


FIG. 10A7

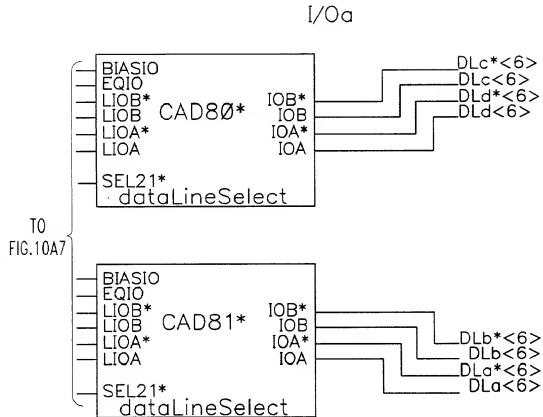


FIG.10A8

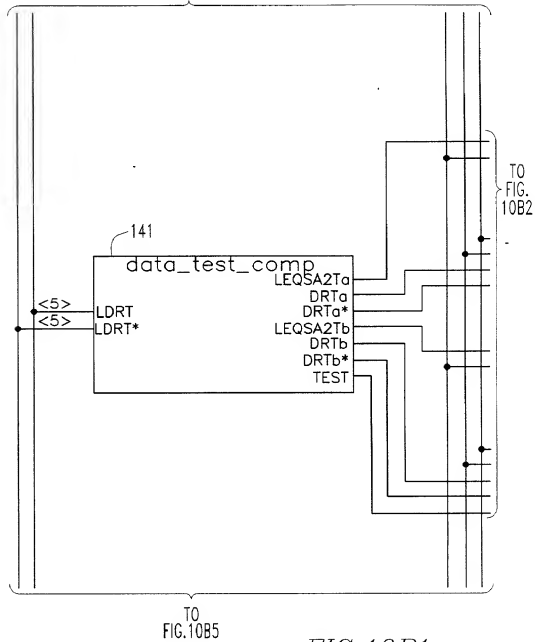
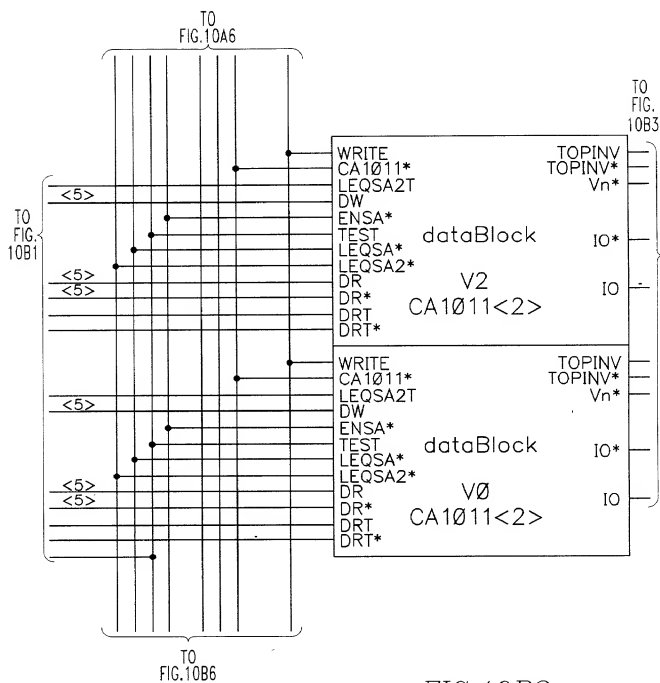
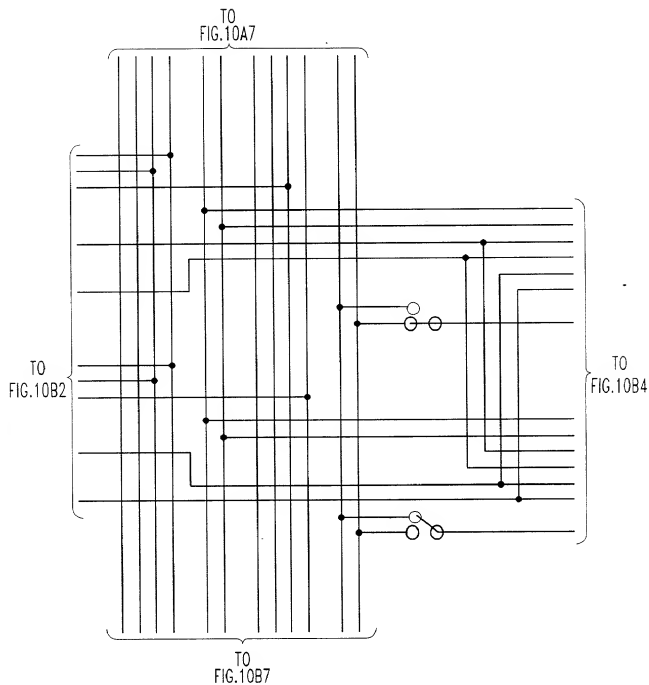
TO
FIG. 10A5

FIG. 10B1



00001520 020001

*FIG. 10B3*

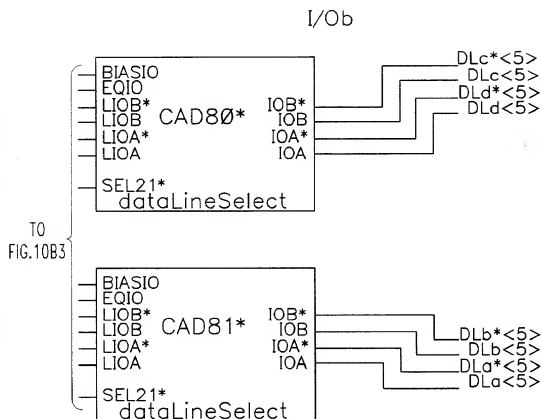


FIG. 10B4

FIG. 10B5

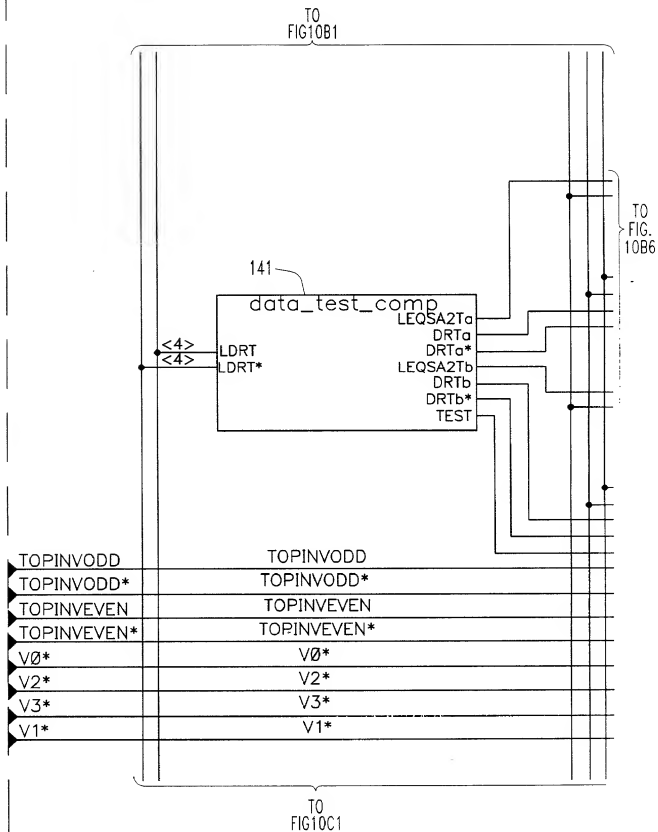


FIG. 10B6

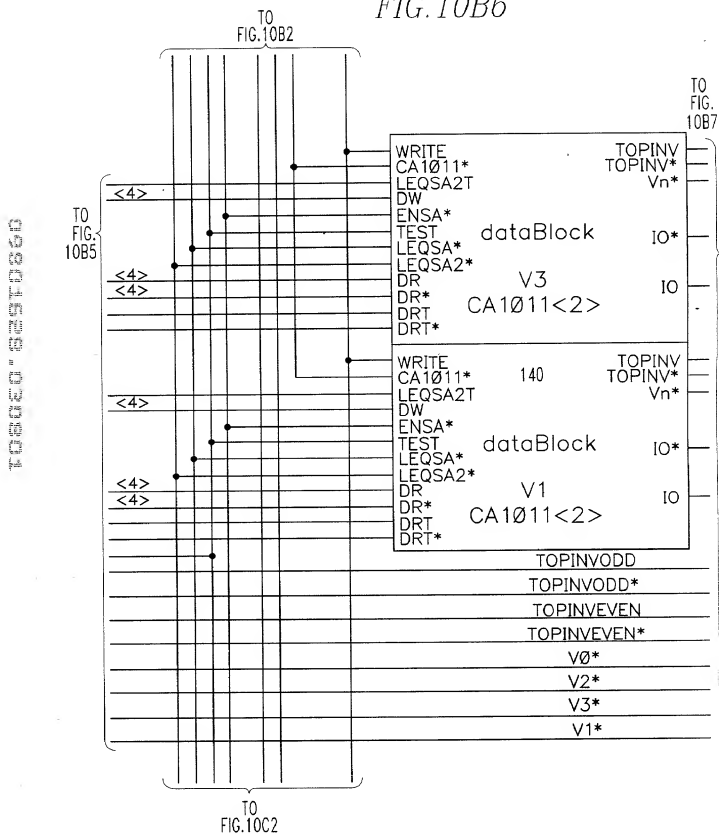


FIG. 10B7

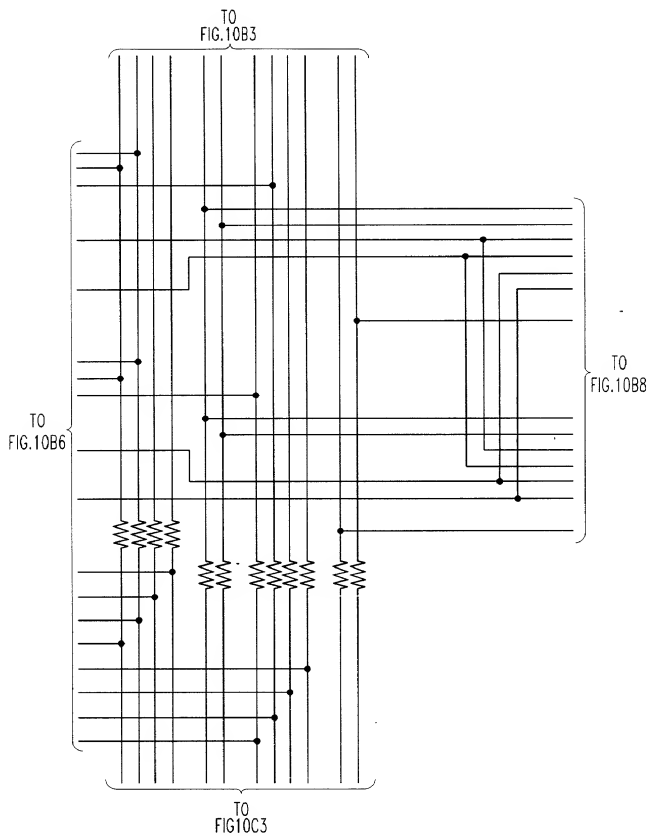
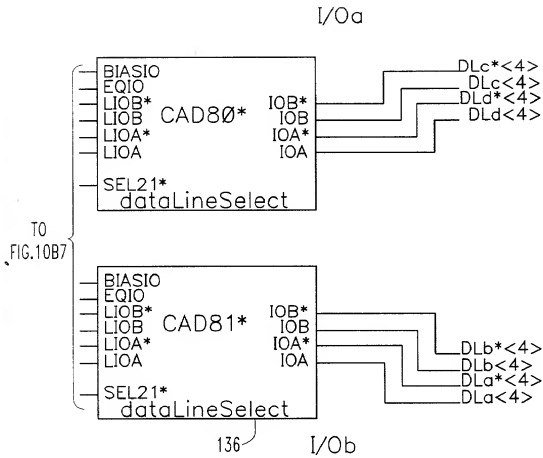


FIG. 10B8



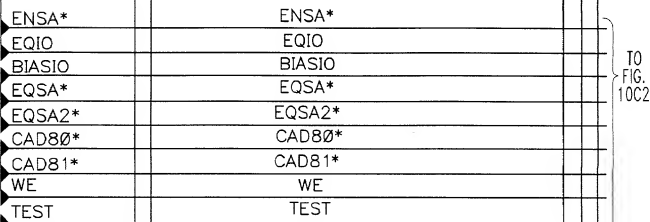
TO
FIG. 10B5TO
FIG. 10C5

FIG. 10C1

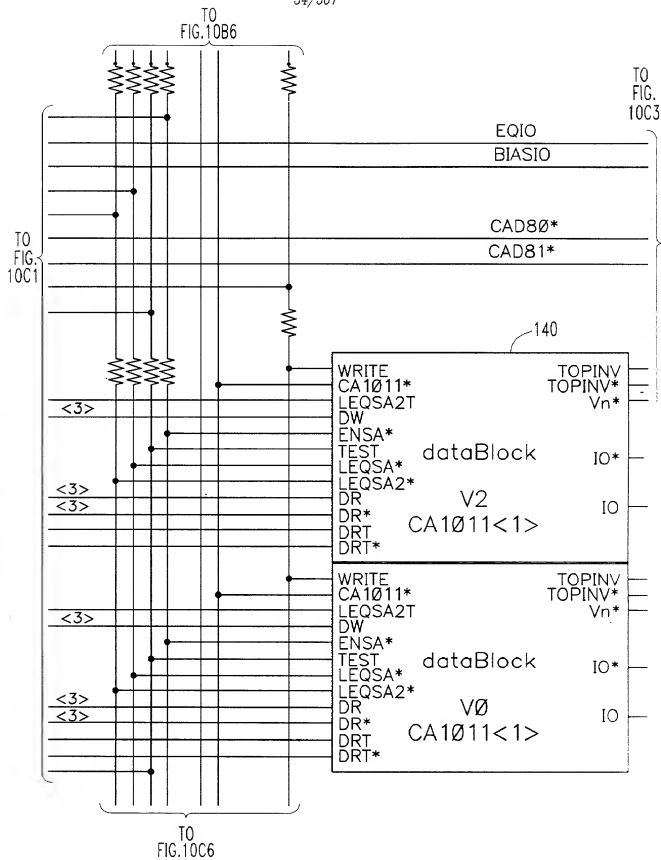


FIG. 10C2

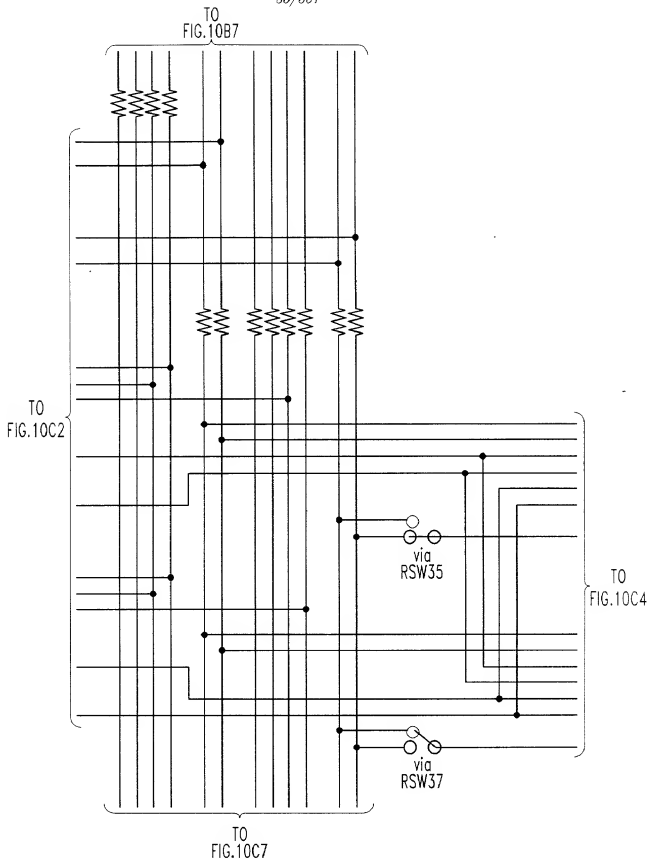
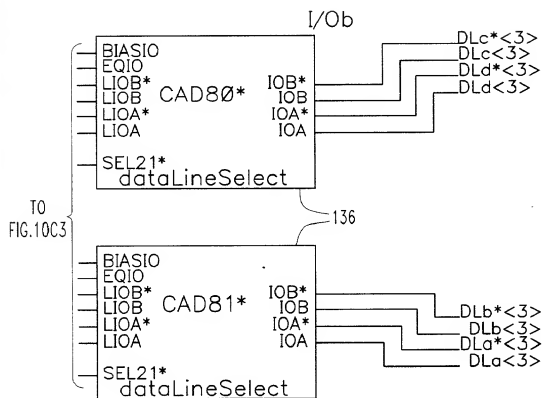


FIG. 10C3

FIG. 10C4



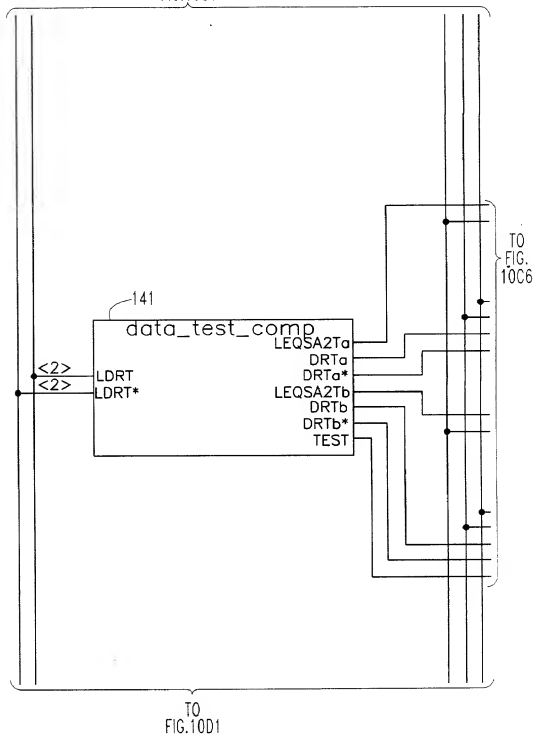
TO
FIG. 10C1

FIG. 10C5

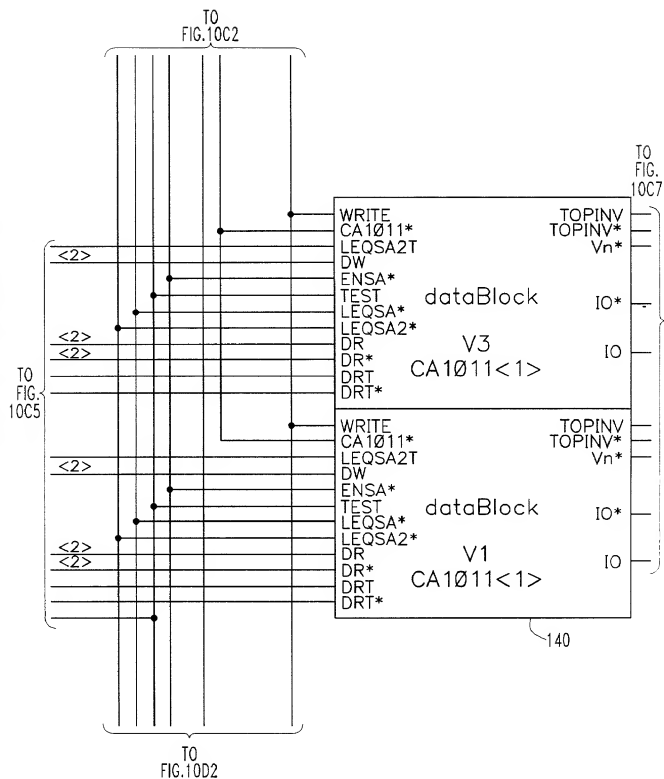


FIG. 10C6

10010101 02010101

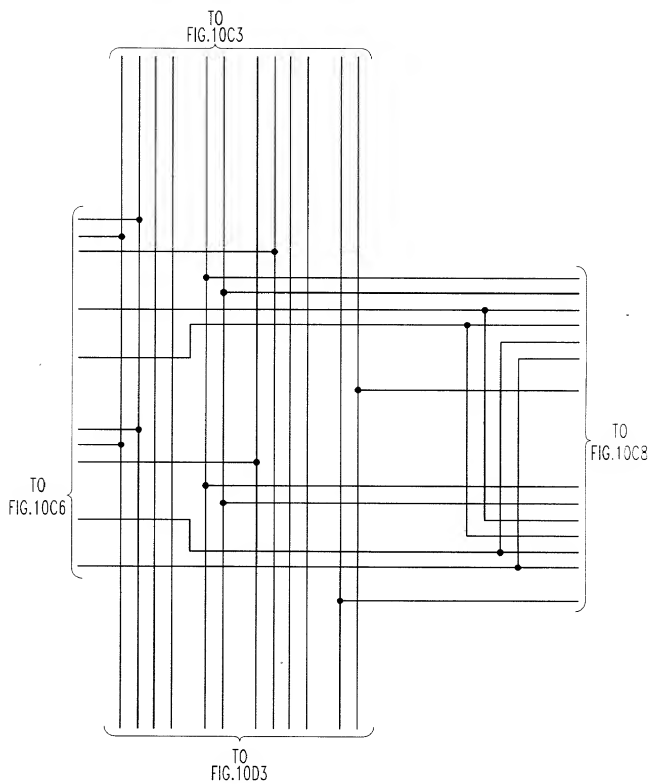


FIG. 10C7

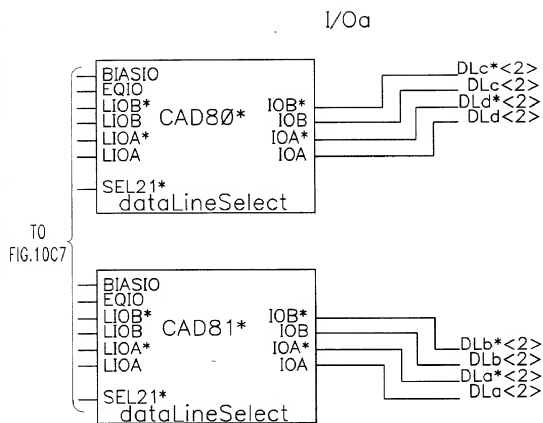


FIG.10C8

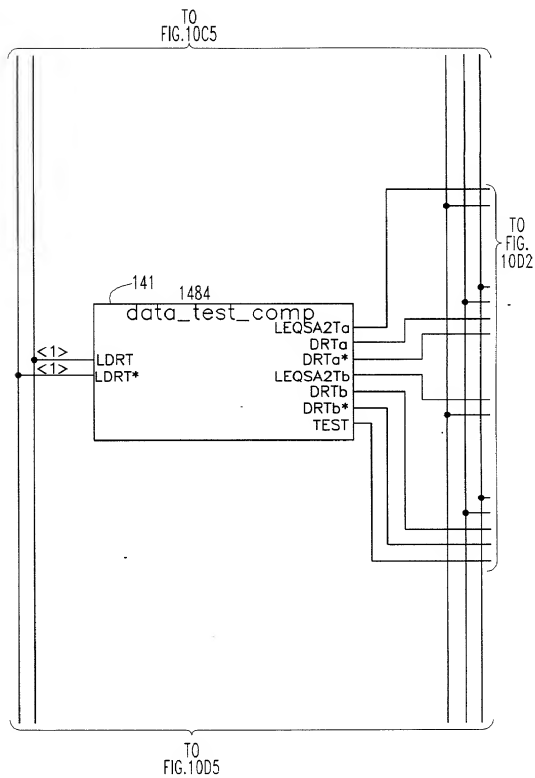


FIG.10D1

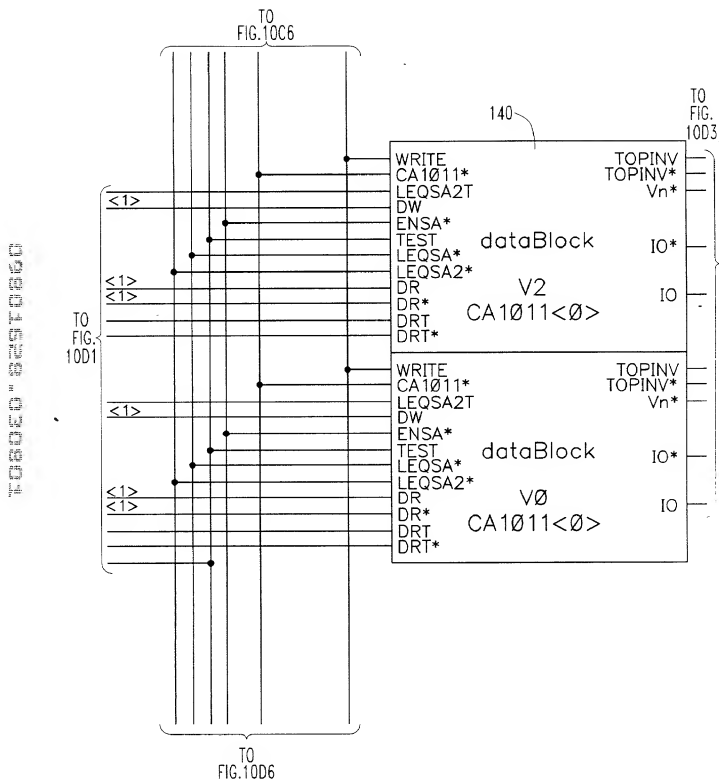
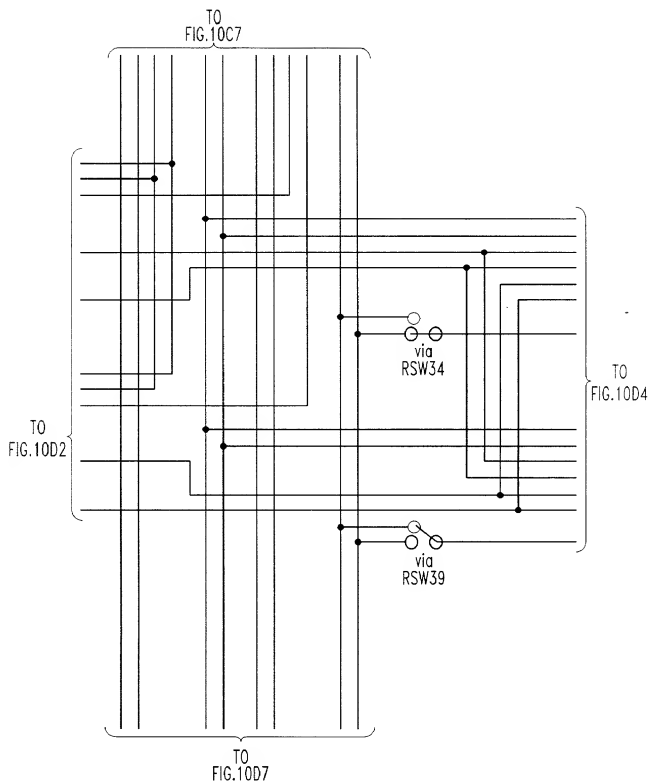


FIG. 10D2

*FIG. 10D3*

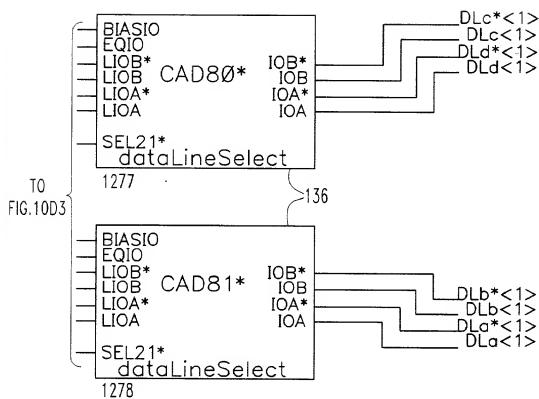
I/O_b

FIG. 10D4

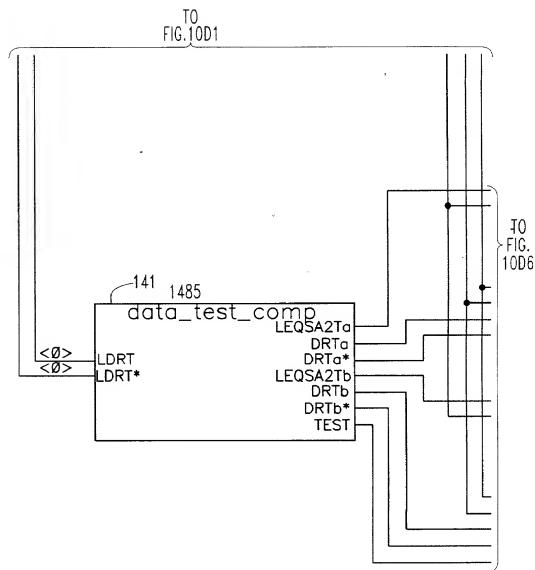


FIG. 10D5

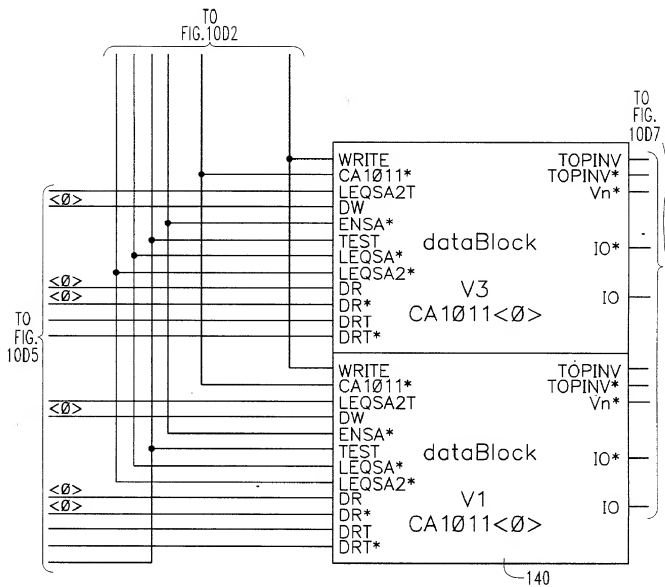


FIG. 10D6

FIG. 10D7

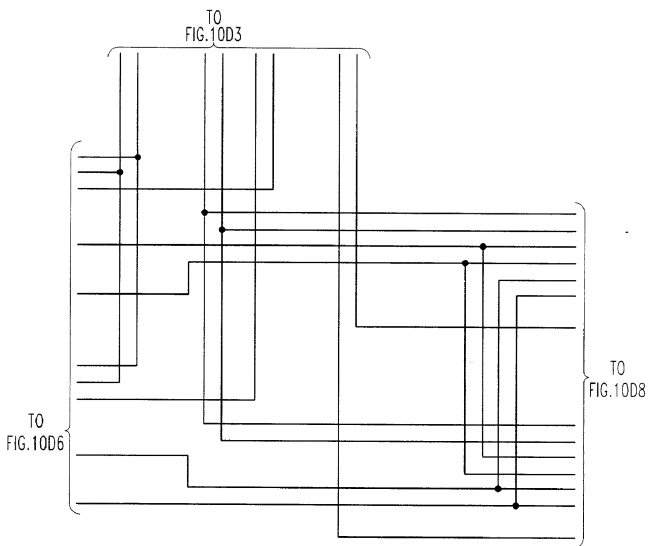


FIG. 10D7

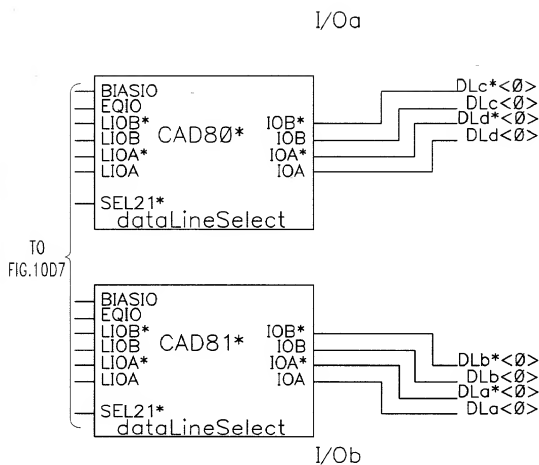


FIG.10D8

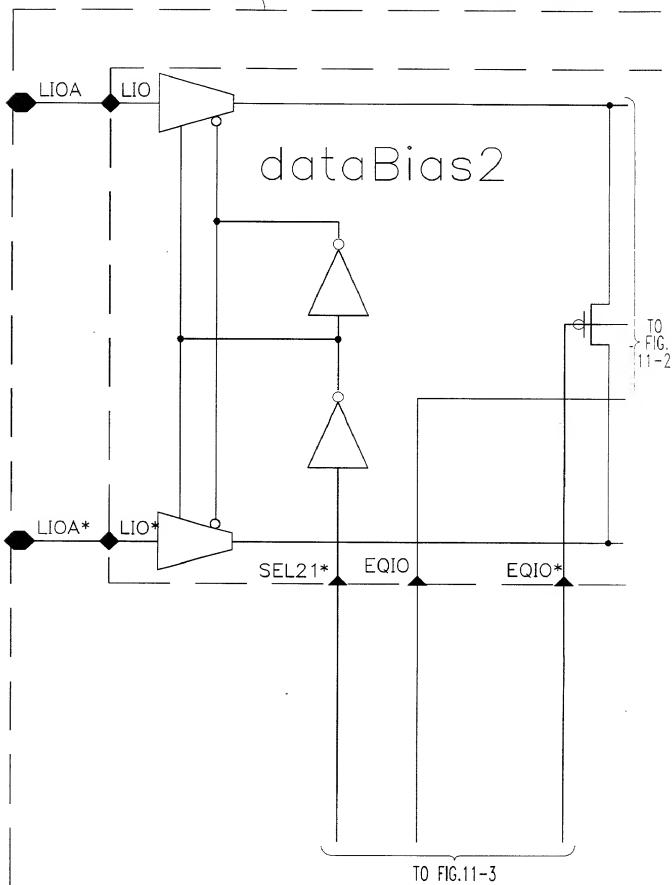
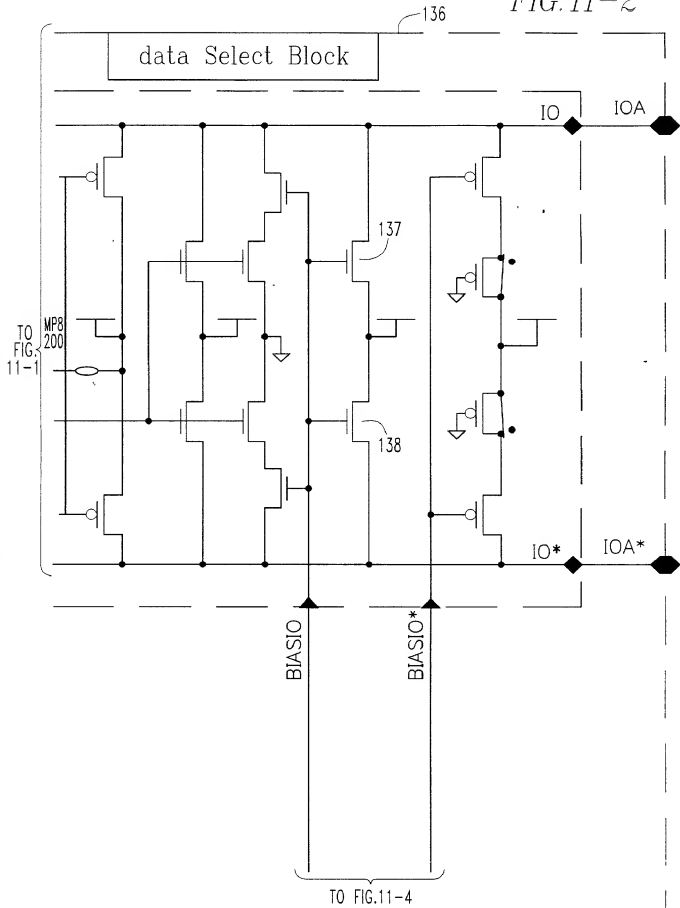


FIG. 11-2



51/367

TO FIG.11-1

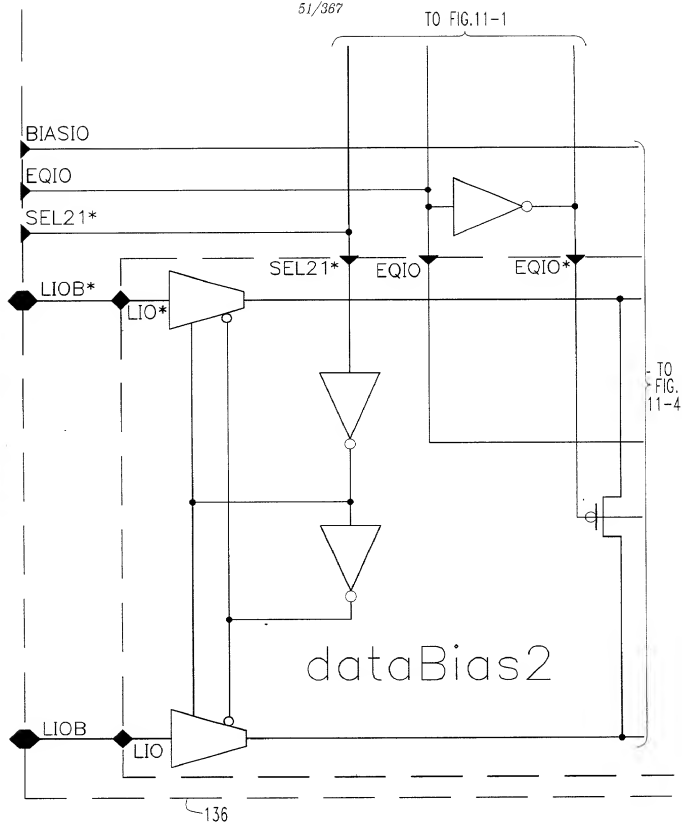


FIG.11-3

52/367

TO FIG. 11-2

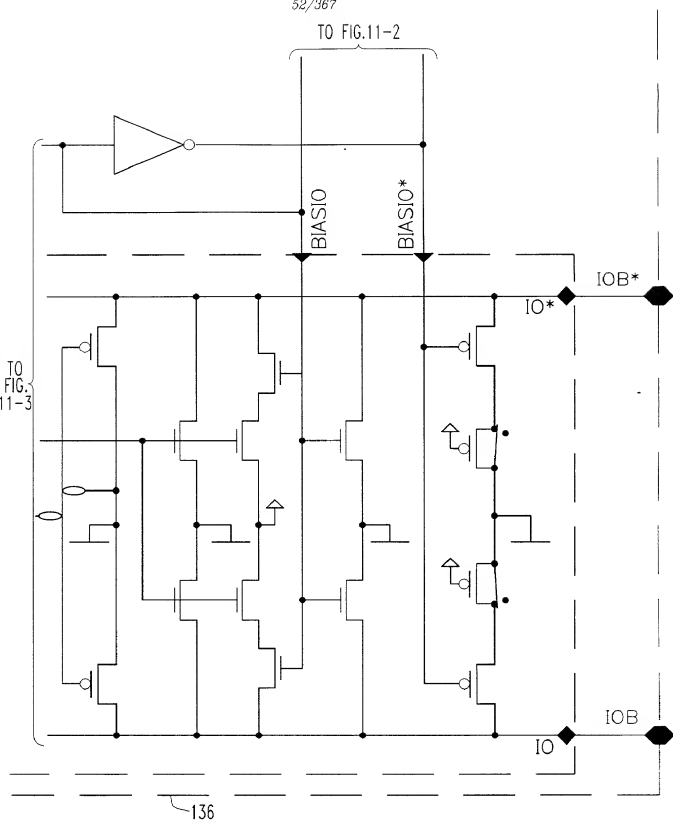
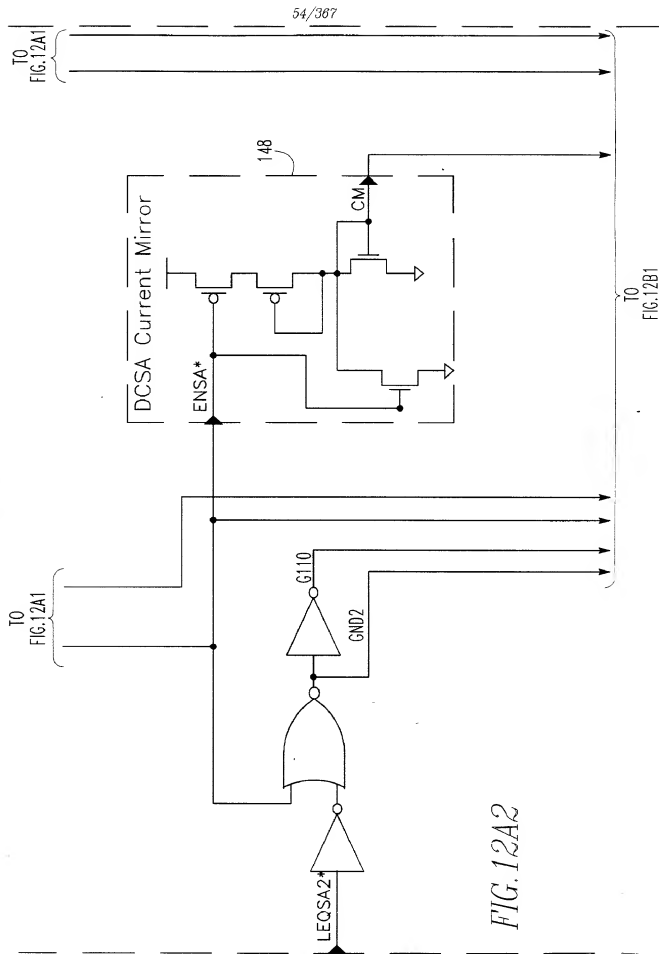


FIG. 11-4



FO8050" 02910860

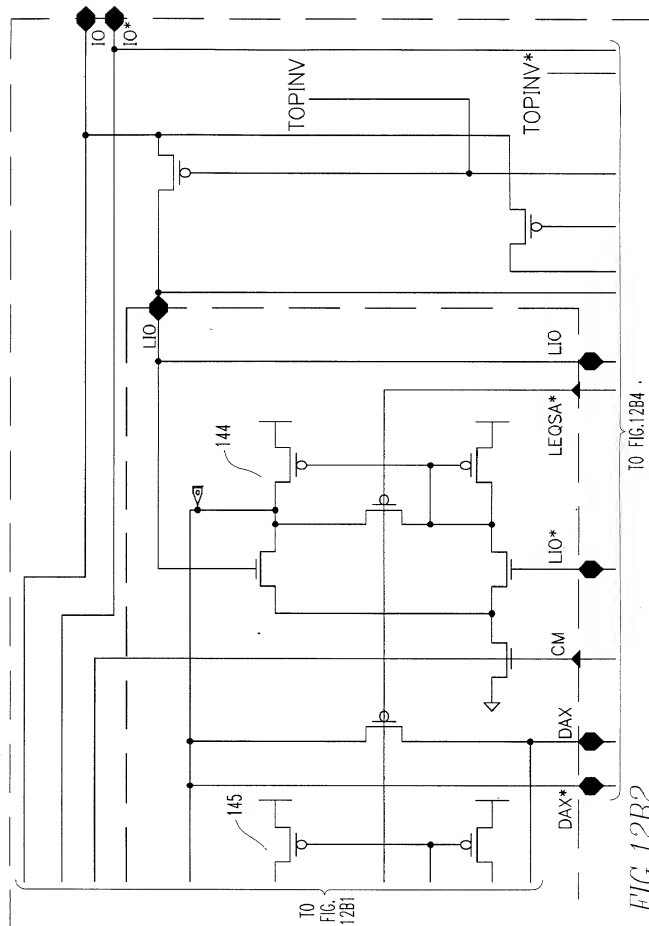


FIG. 12B2

TO FIG. 12B4 .

TO
FIG.
12B1

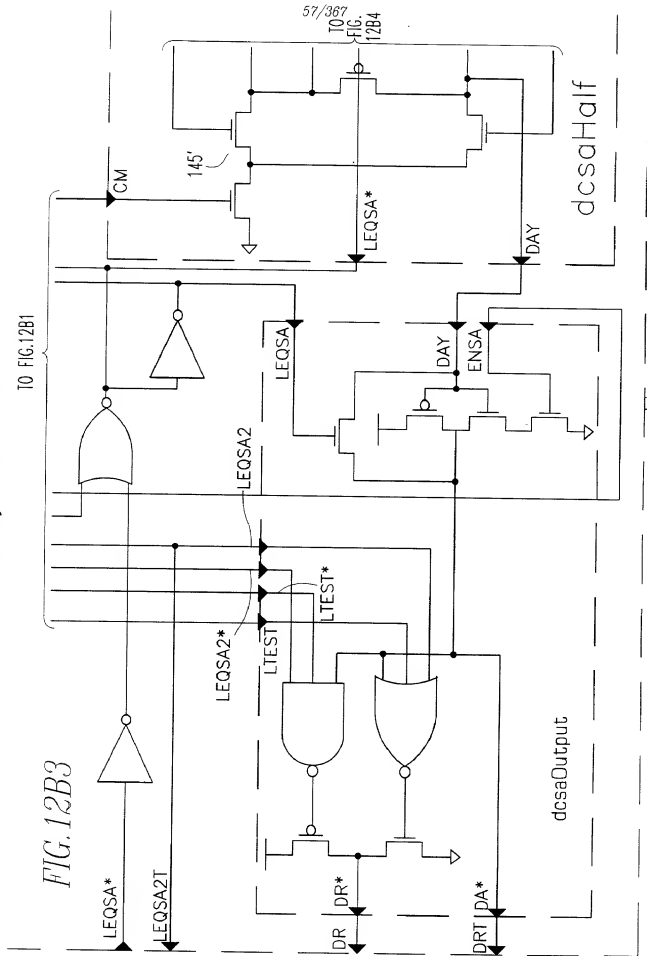
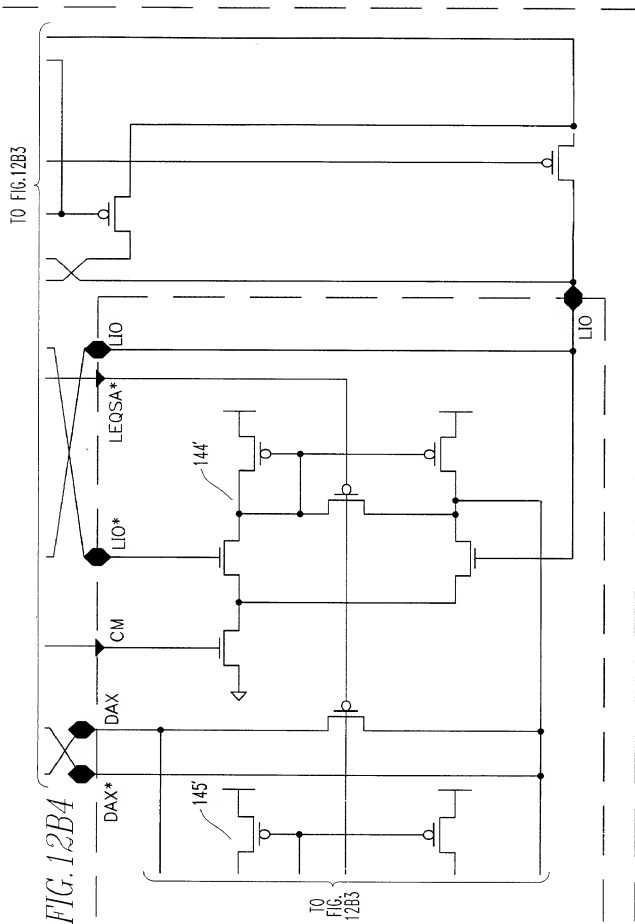
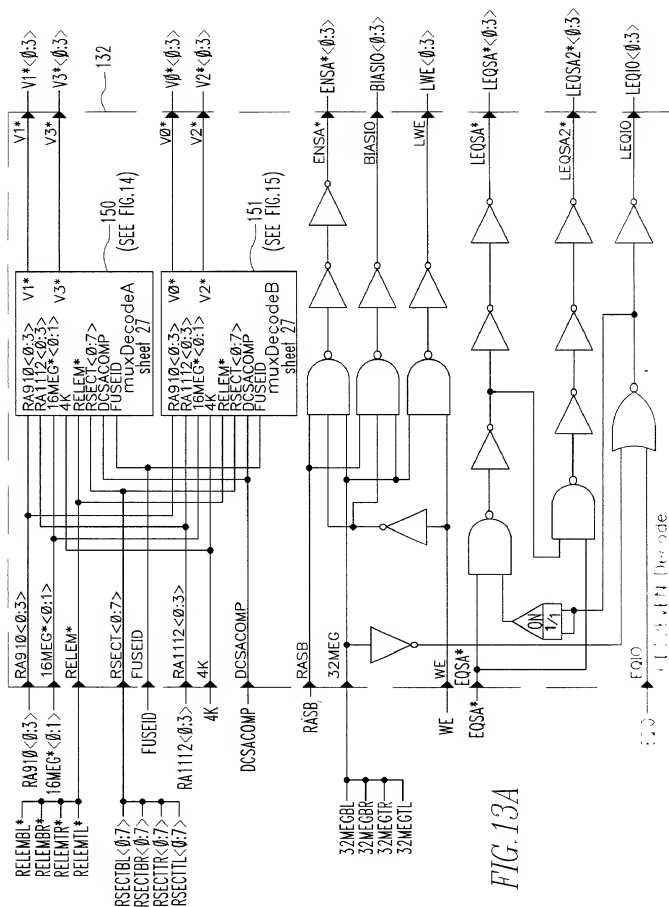
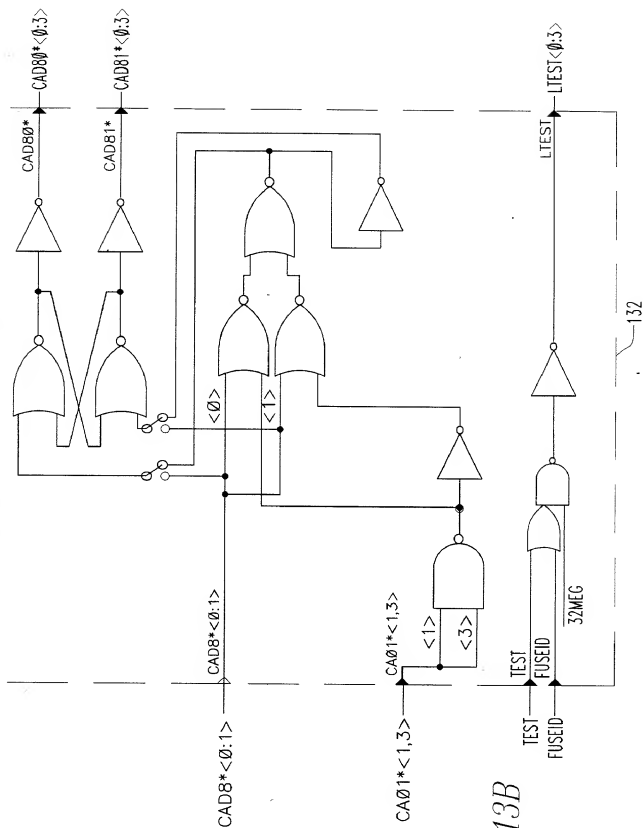


FIG. 12B4







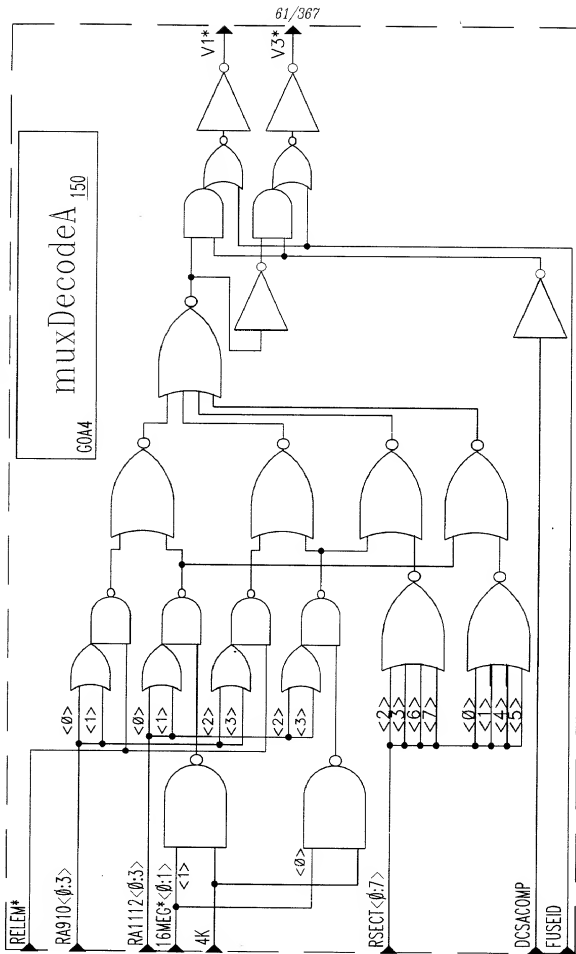
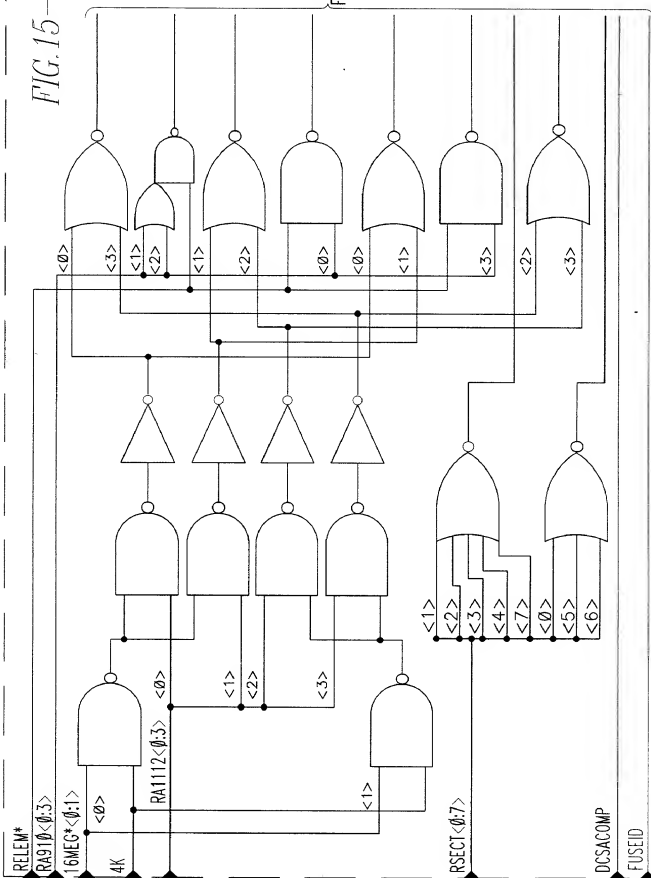


FIG.14

FIG. 15-1



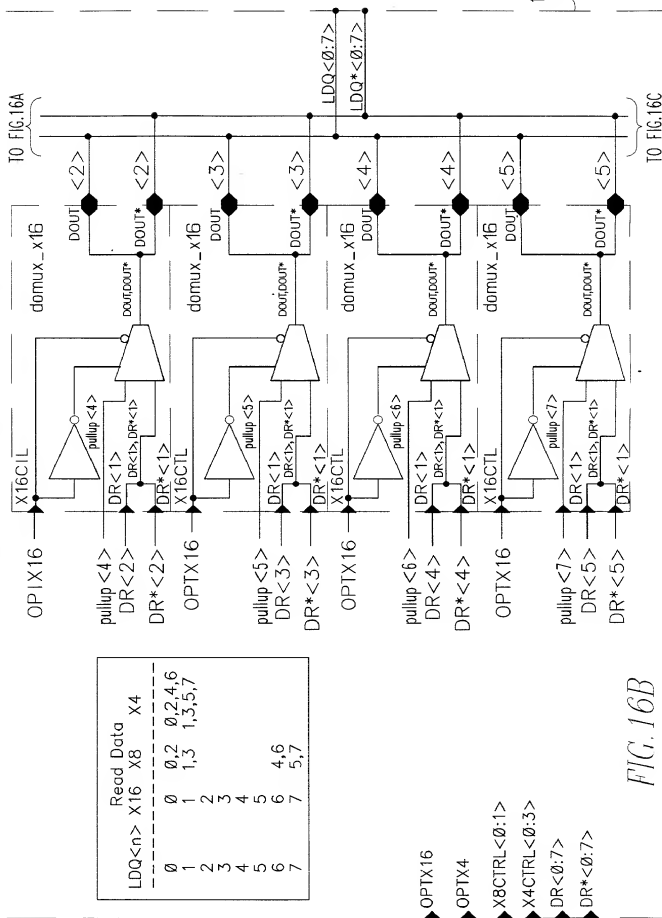
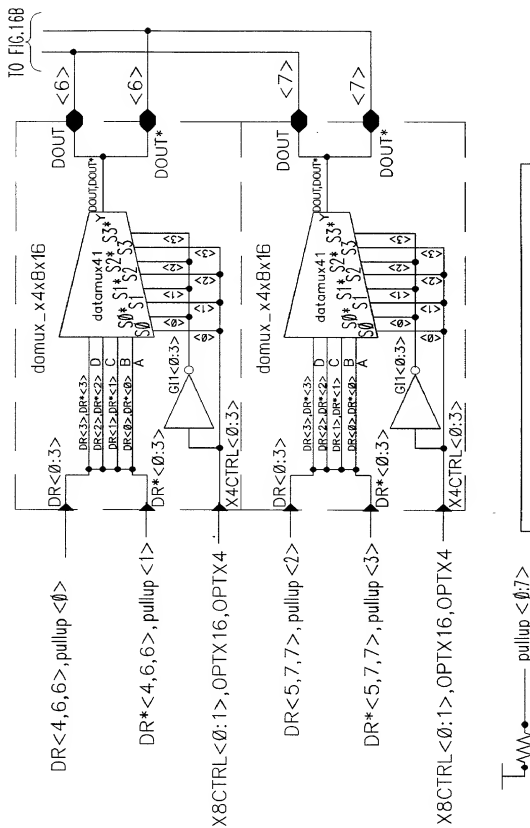


FIG. 16B



dataReadMux

FIG. 16C

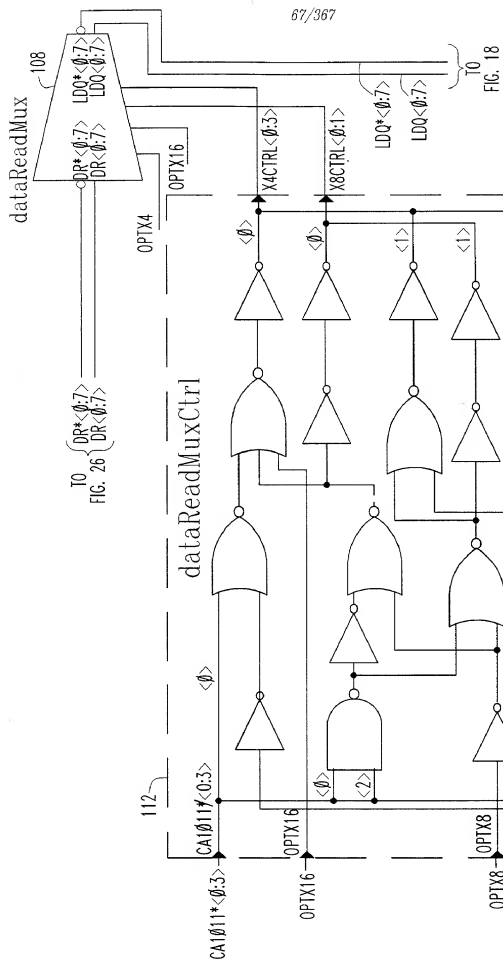
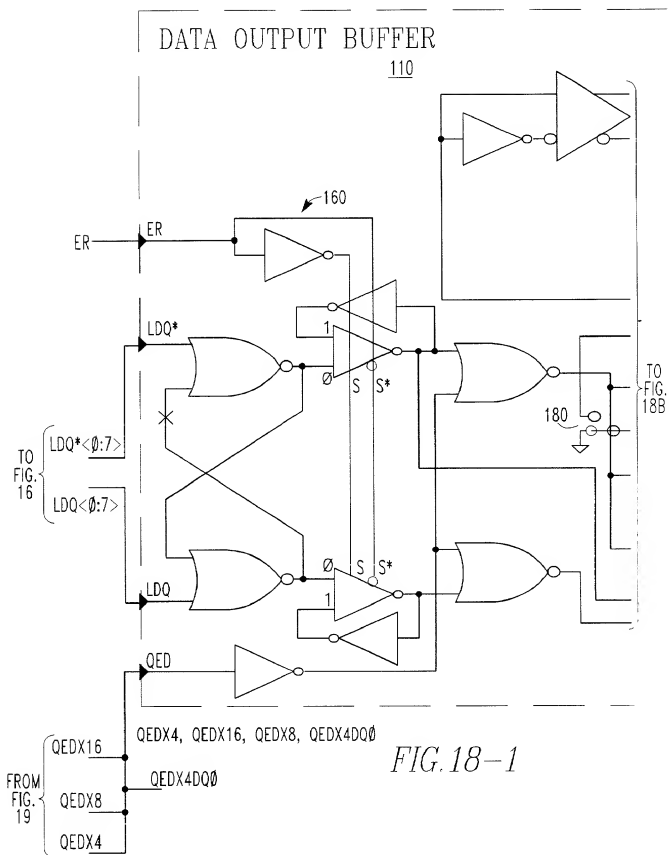


FIG. 17



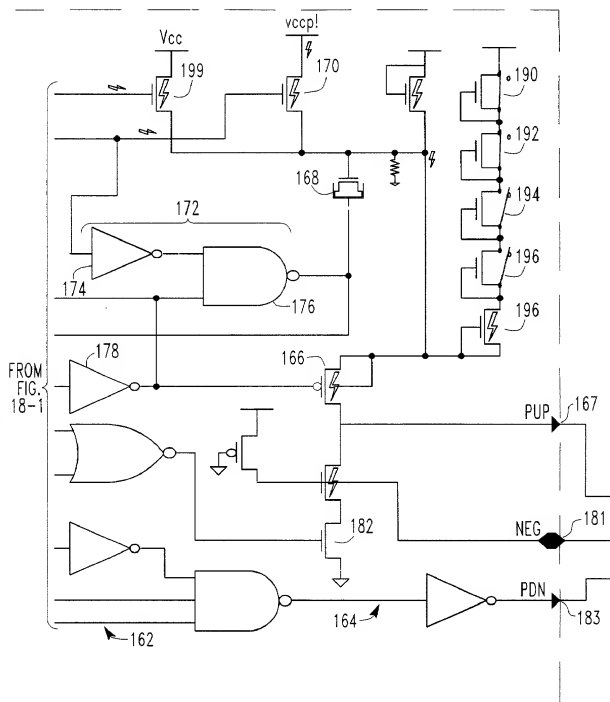


FIG. 18-2

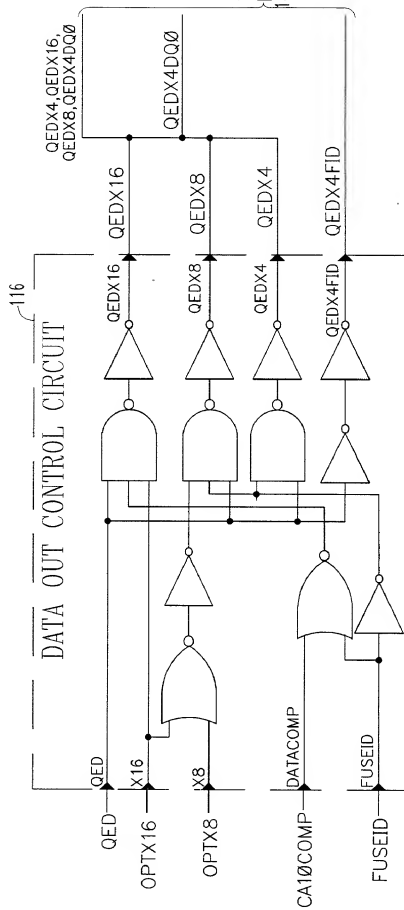


FIG. 19

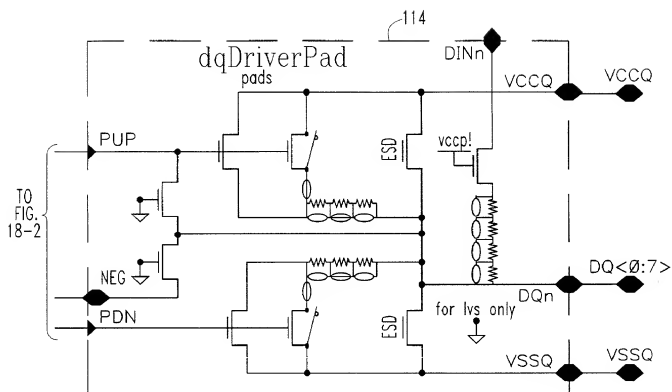


FIG. 20

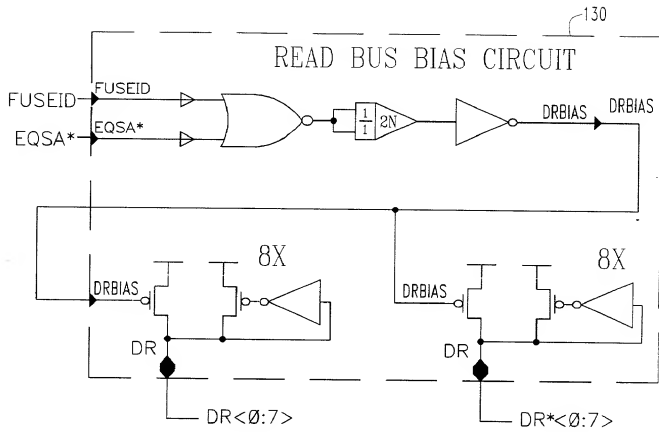
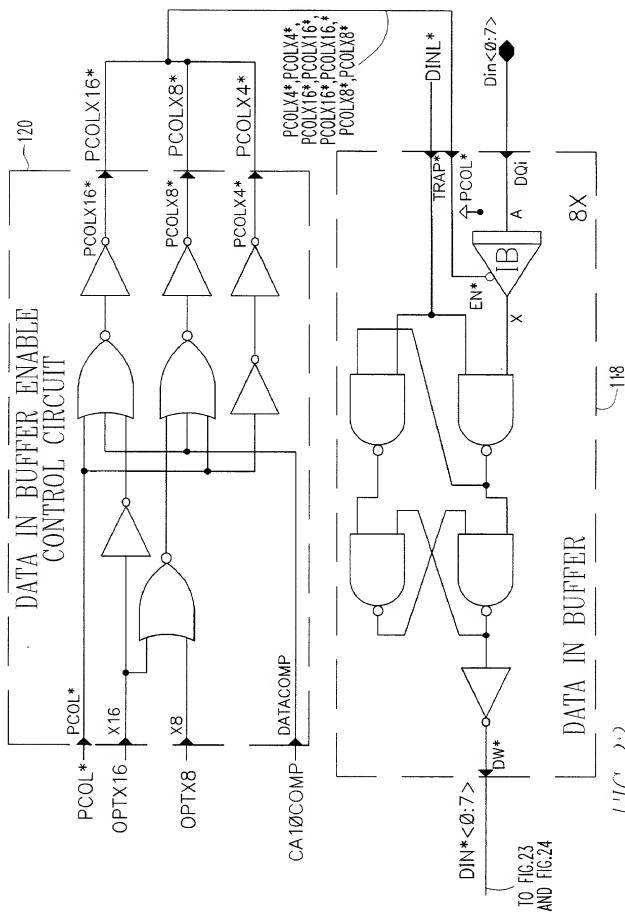
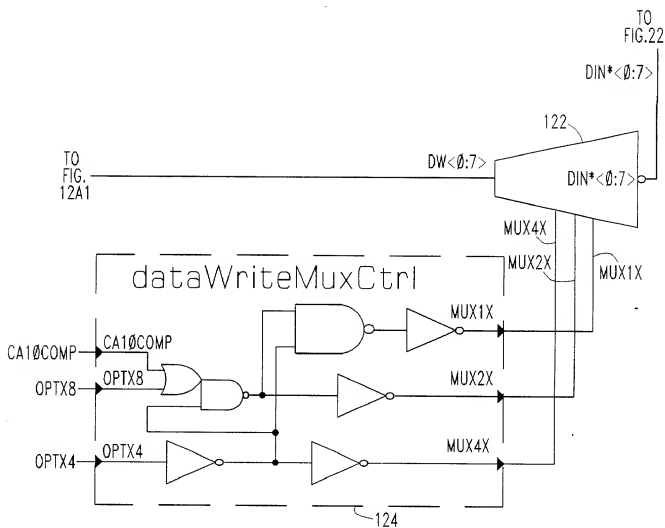
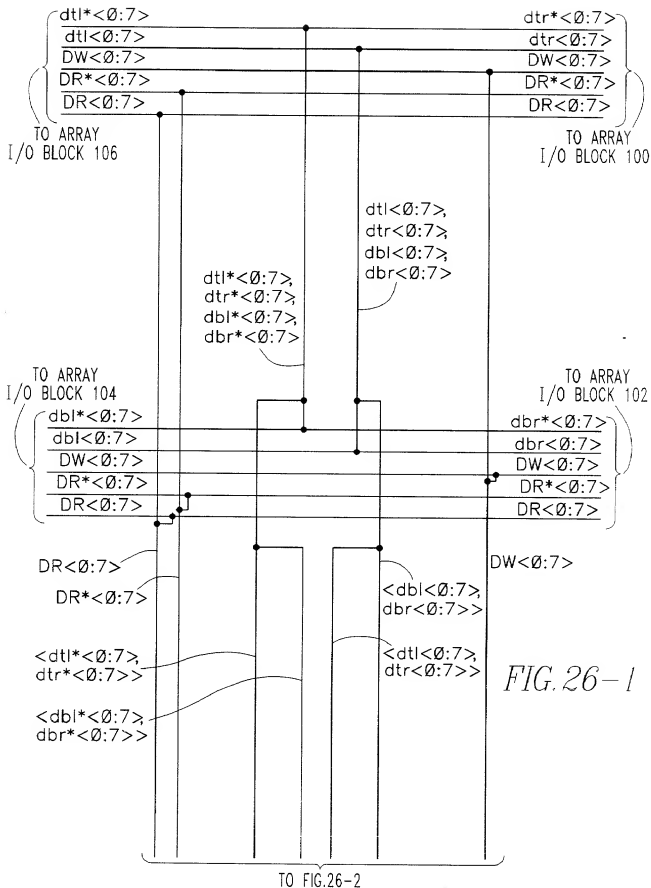


FIG. 21









FROM FIG. 26-1

READ/WRITE
BUStdl* <0:7>
tdr* <0:7>

tdl <0:7>

tdl <0:7>
tdr <0:7>

tdr* <0:7>

tdr <0:7>

tdl* <0:7>

TDL* <0:7>
TDL <0:7>TDR* <0:7>
TDR <0:7>

128 (SEE FIG. 27)

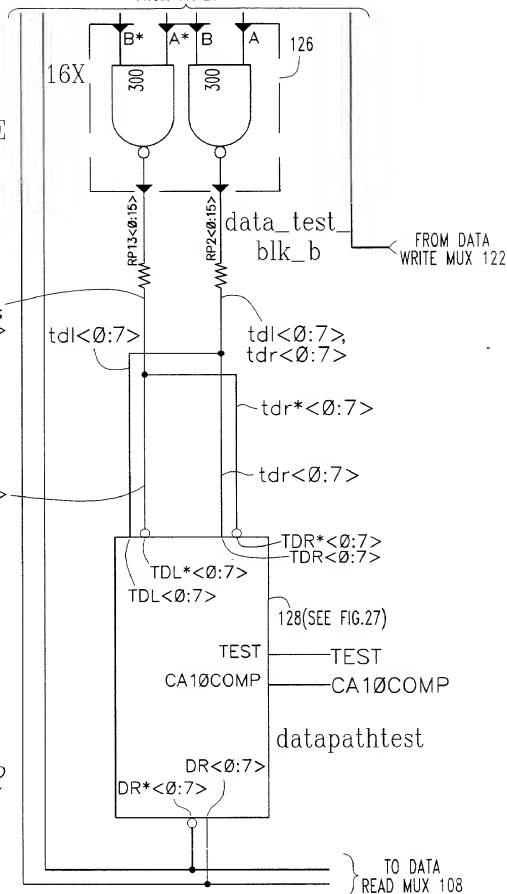
TEST

CA10COMP

datapath test

DR* <0:7>
DR <0:7>TO DATA
READ MUX 108

FIG. 26-2



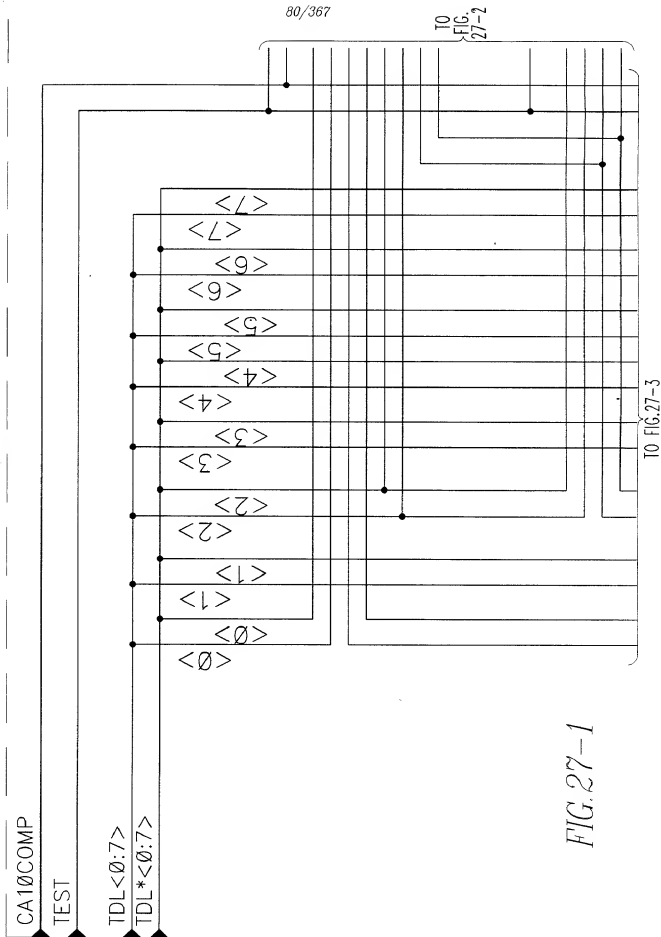
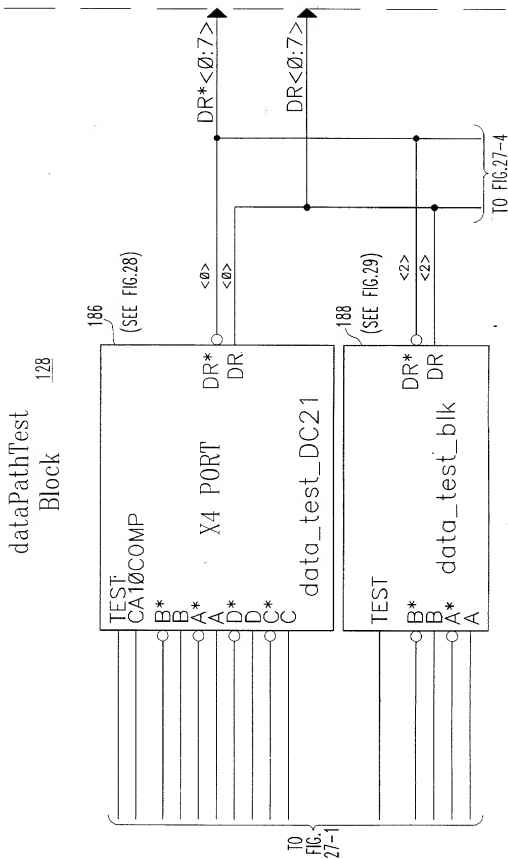


FIG. 27-1

FIG. 27-2



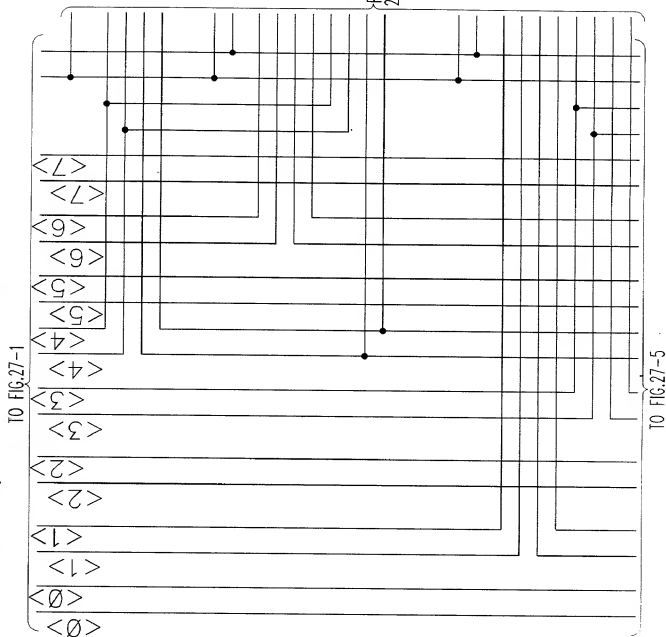
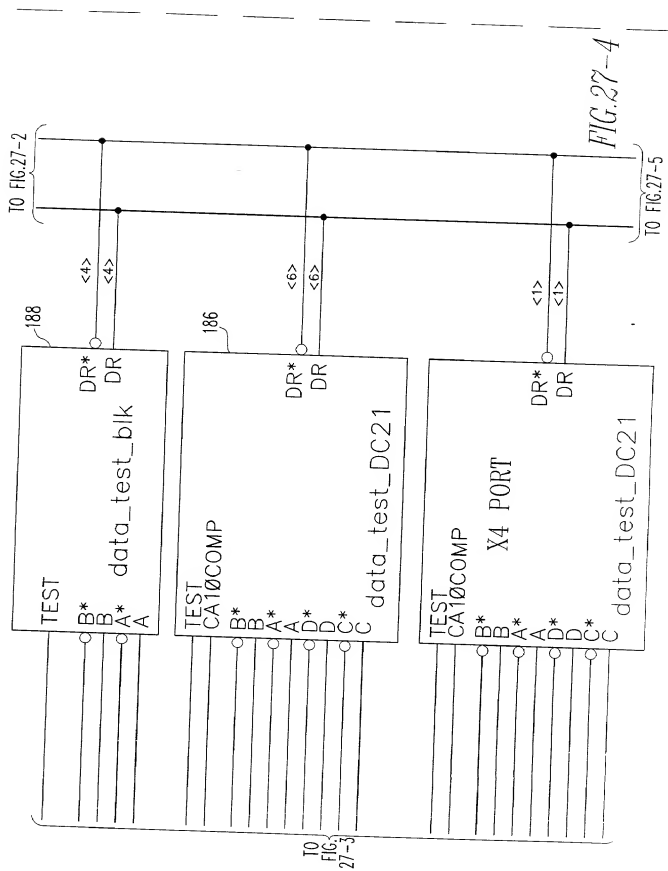
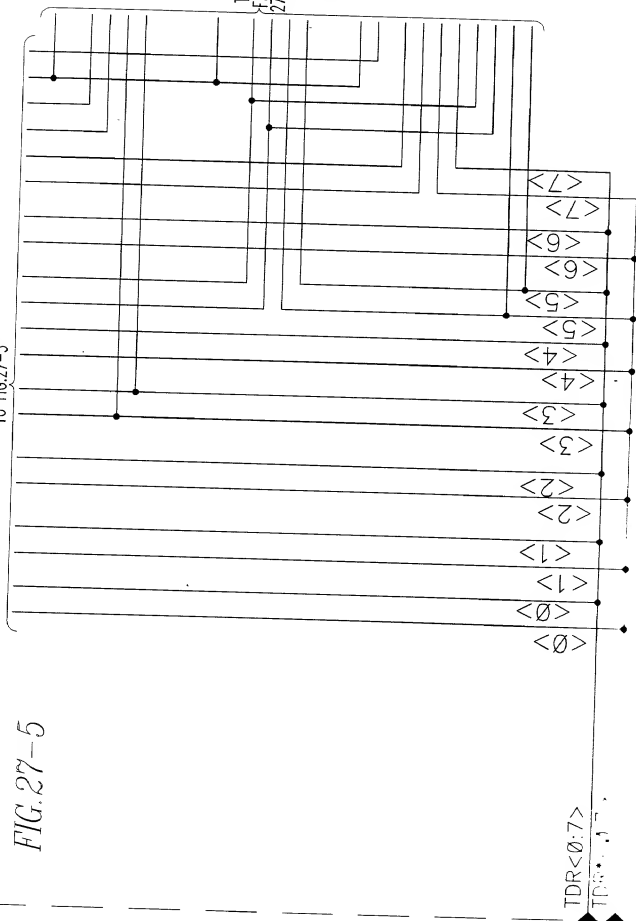


FIG 27-3



TO FIG. 27-3

FIG. 27-5



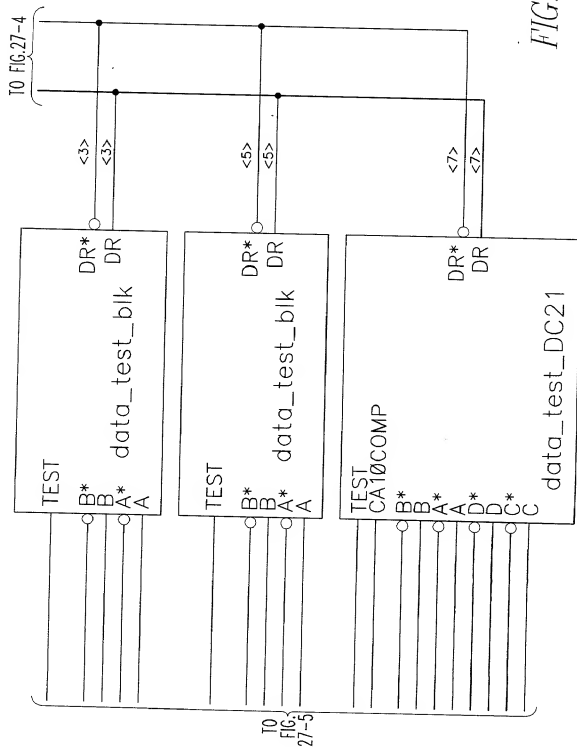


FIG. 27-6

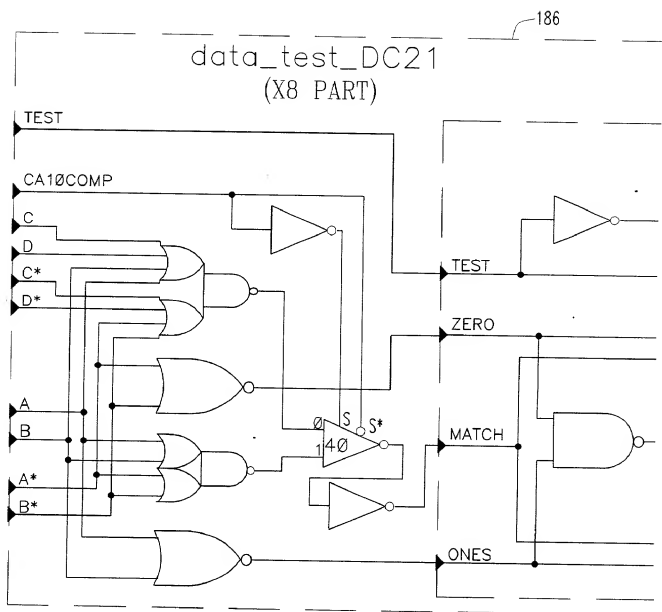


FIG. 28-1

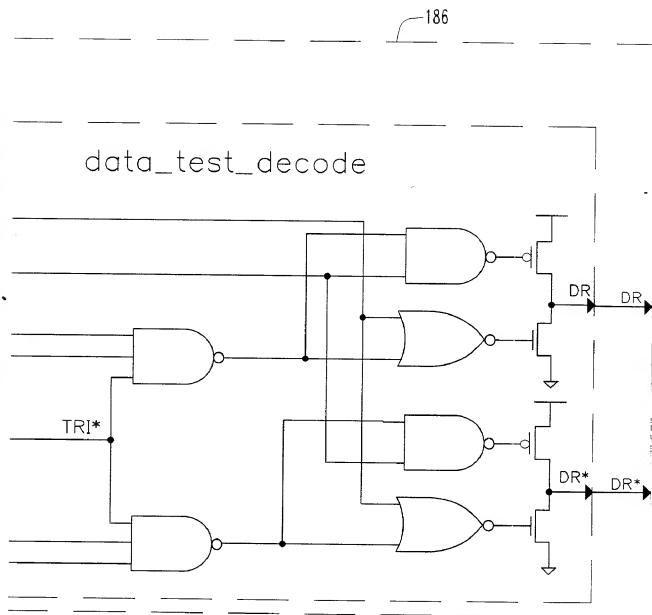


FIG. 28-2

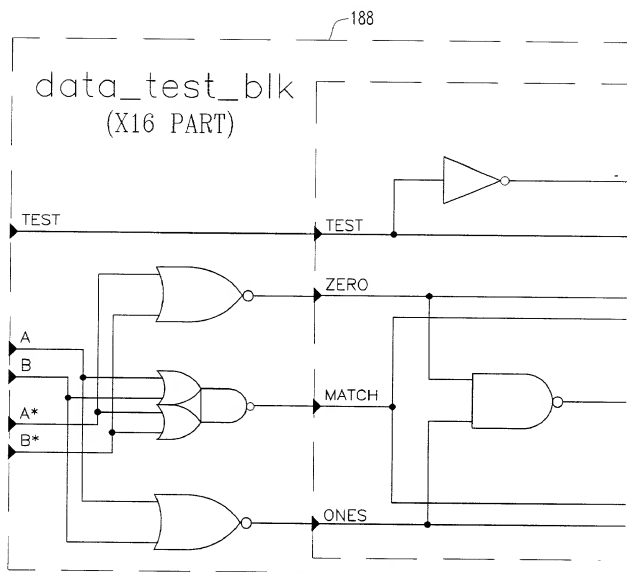


FIG. 29-1

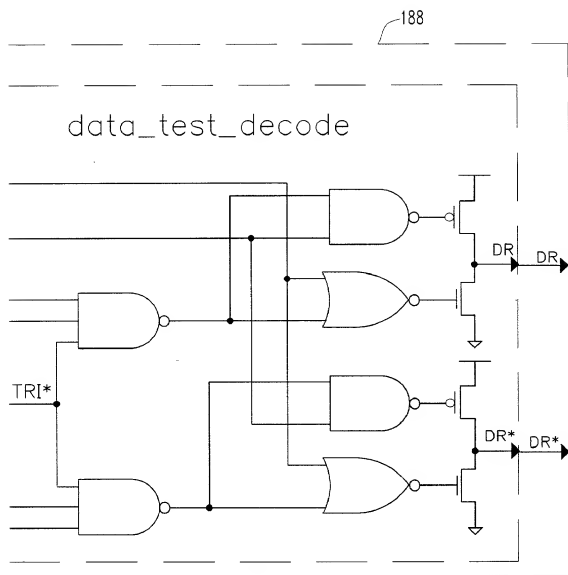


FIG. 29-2

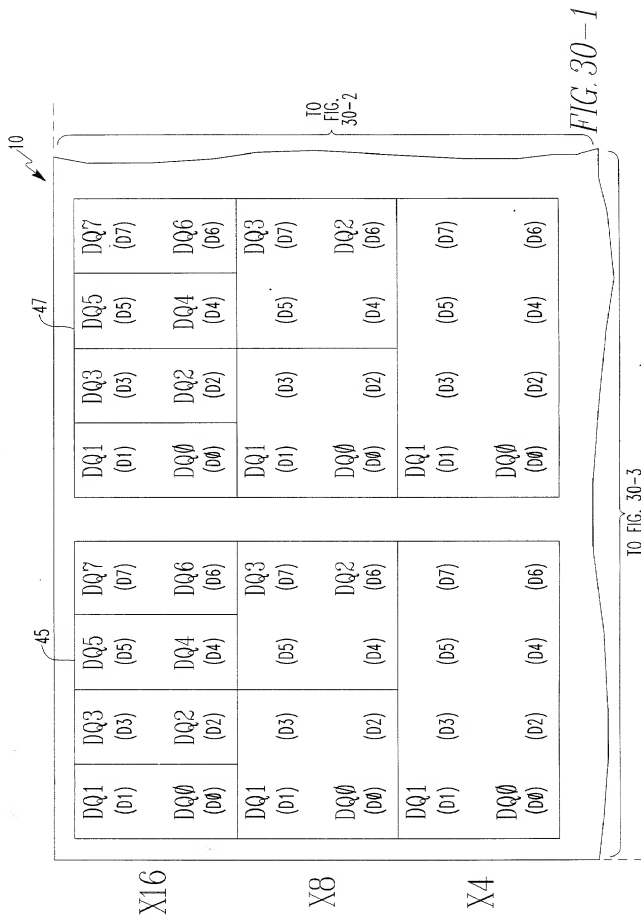
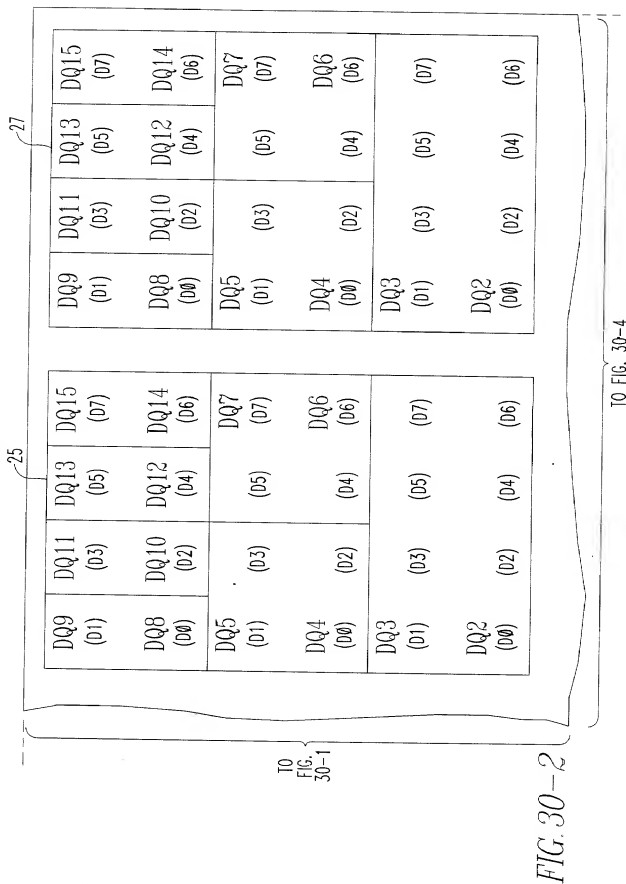


FIG. 30-3



TO FIG. 30-1

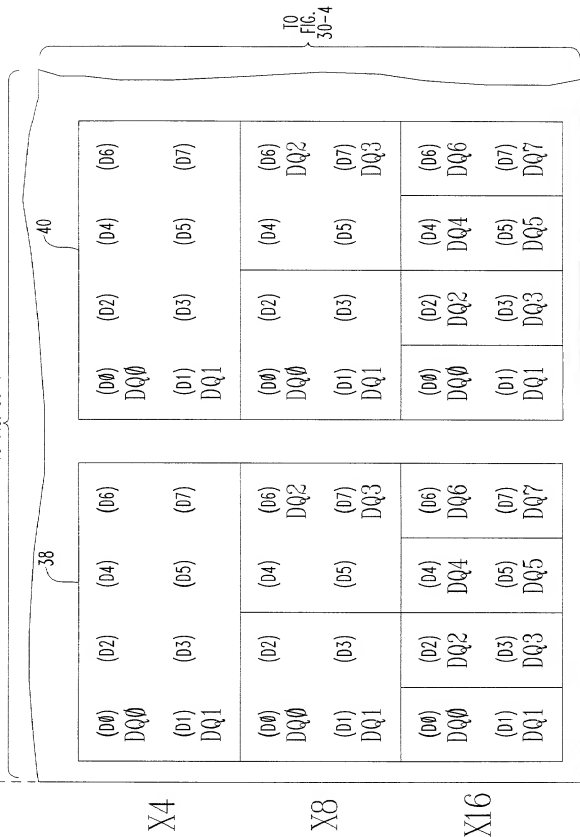


FIG. 30-3

1000000-82910860

TO FIG. 30-2

31			33			
(00) DQ2	(02)	(04)	(06)	(02)	(04)	(06)
(01) DQ3	(03)	(05)	(07)	(03)	(05)	(07)
(00) DQ4	(02)	(04)	(06)	(02)	(04)	(06)
(01) DQ5	(03)	(05)	(07)	(03)	(05)	(07)
(00) DQ8	(02)	(04)	(06)	(02)	(04)	(06)
(01) DQ9	(03)	(05)	(07)	(03)	(05)	(07)

(00) DQ2	(02)	(04)	(06)	(02)	(04)	(06)
(01) DQ3	(03)	(05)	(07)	(03)	(05)	(07)
(00) DQ4	(02)	(04)	(06)	(02)	(04)	(06)
(01) DQ5	(03)	(05)	(07)	(03)	(05)	(07)
(00) DQ8	(02)	(04)	(06)	(02)	(04)	(06)
(01) DQ9	(03)	(05)	(07)	(03)	(05)	(07)

TO
FIG.
30-3

FIG. 30-1

T0 FIG. 31A1

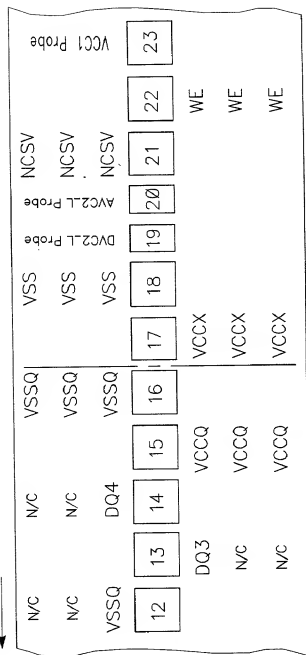
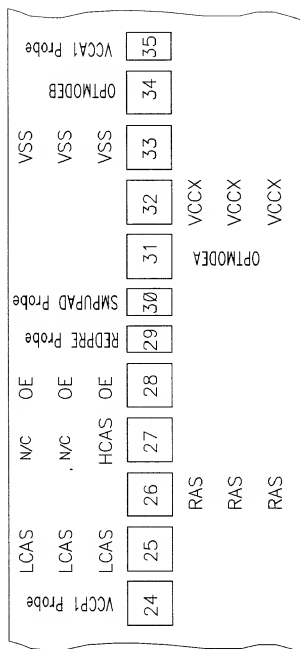


FIG. 31A2



TO FIG. 31B2

FIG. 31B1

[illegible]

FIG. 31C2

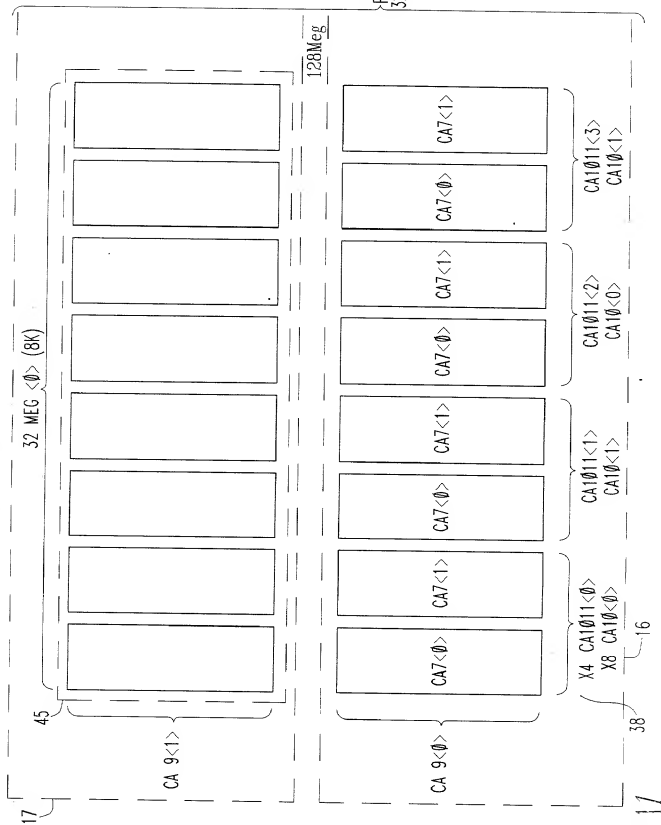
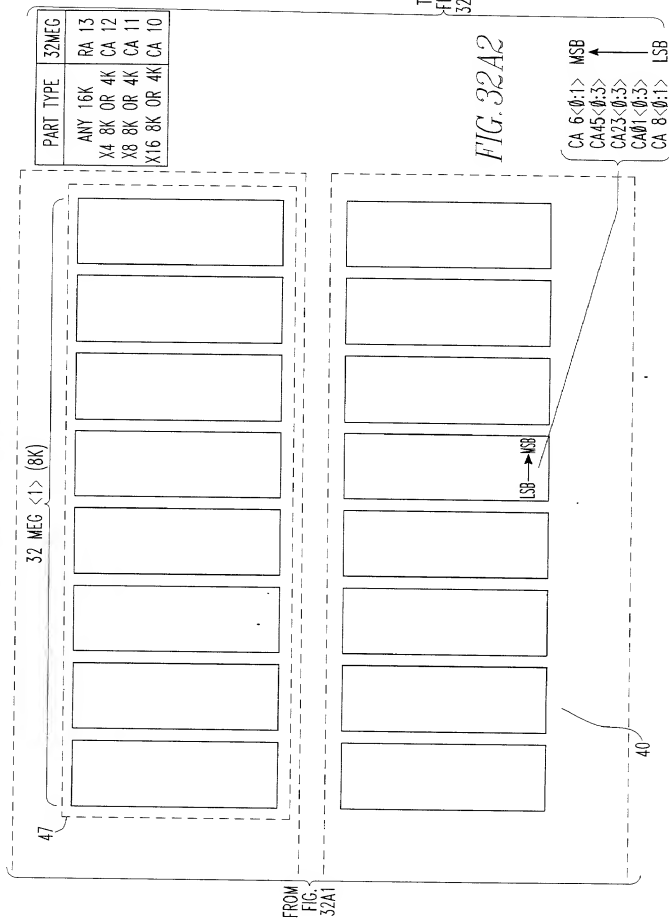


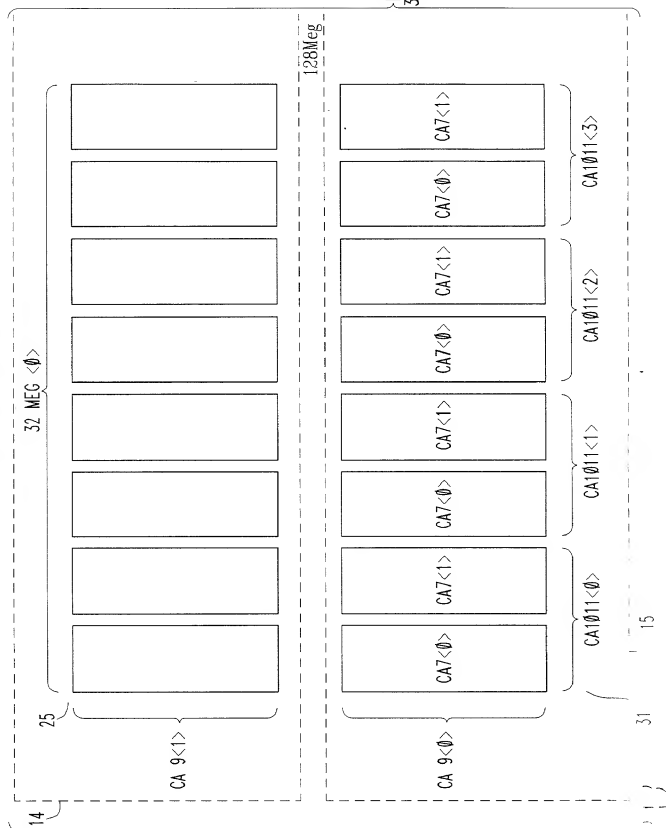
FIG. 32A1

108050" 82910860



FROM
FIG.
32A2

108020" 22310860



FROM
FIG.
32A3

108020-82510860

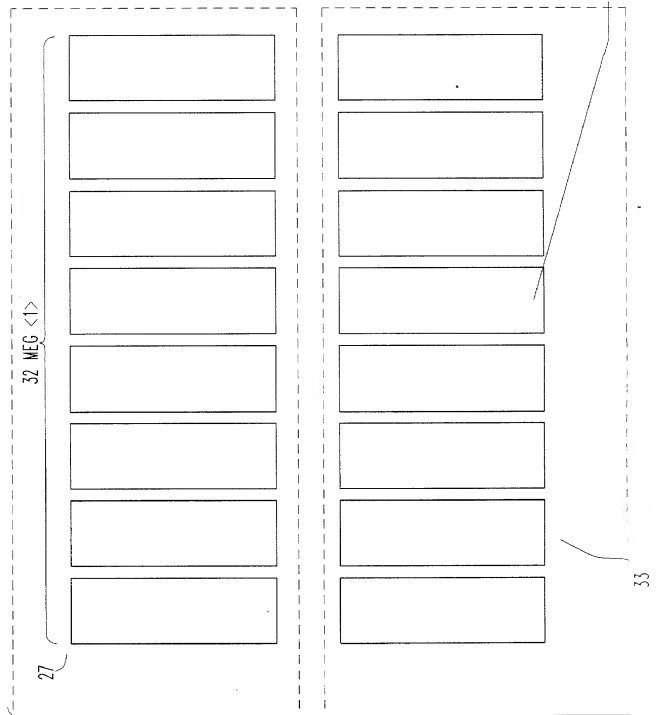


FIG. 32A4

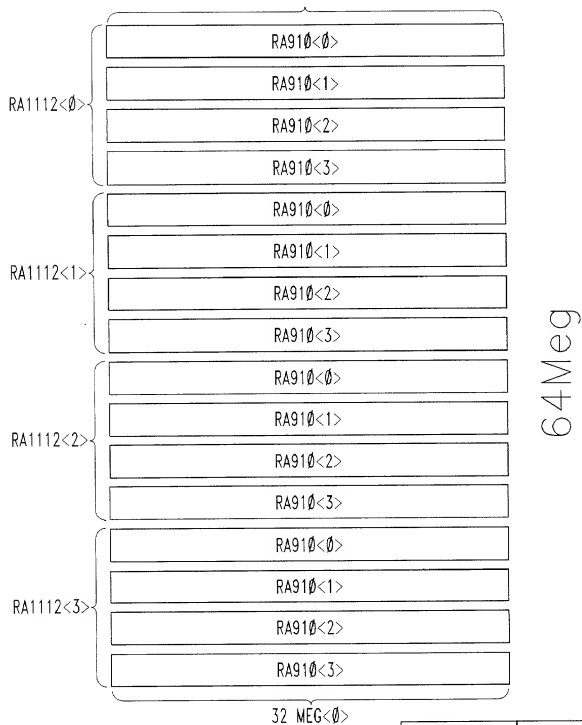


FIG. 32B1

PART TYPE	32MEG
ANY 16K	RA_13
X4 8K OR 4K	CA_12
X8 8K OR 4K	CA_11
X16 8K OR 4K	CA_10

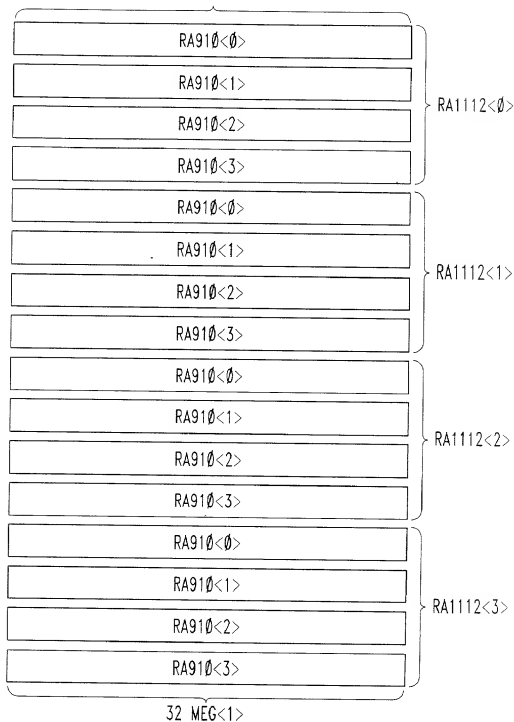
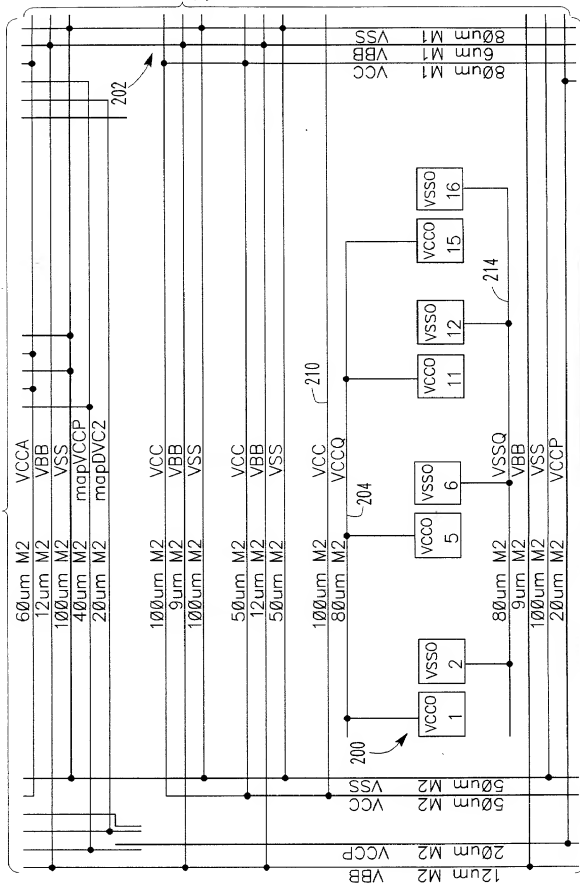


FIG. 32B2



FIG. 33A1

FROM FIG. 33A1



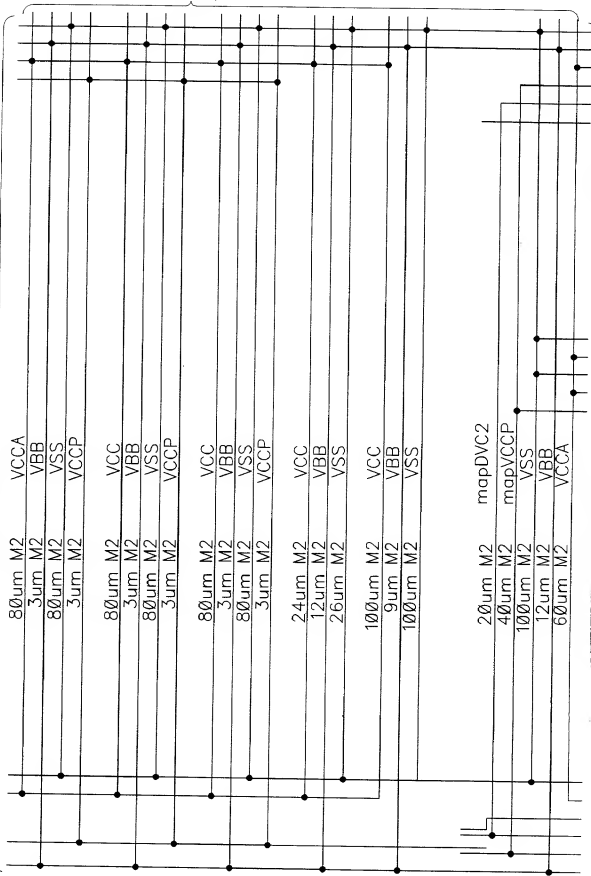
TO
FIG.
33A3

107/367

TO FIG. 33A3

FIG. 33A2

FROM FIG. 33A2



TO
FIG.
33B5

108/367

TO FIG. 33A4

FIG. 33A3

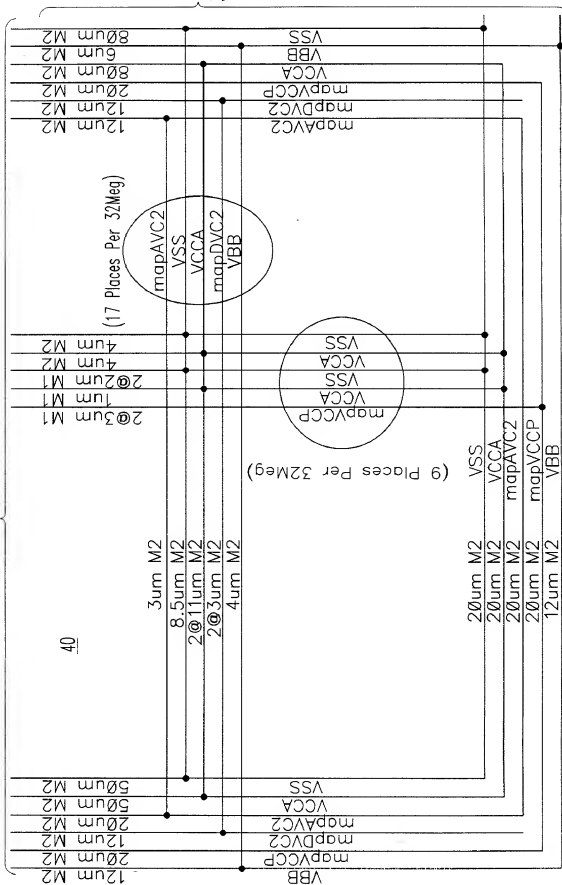
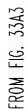
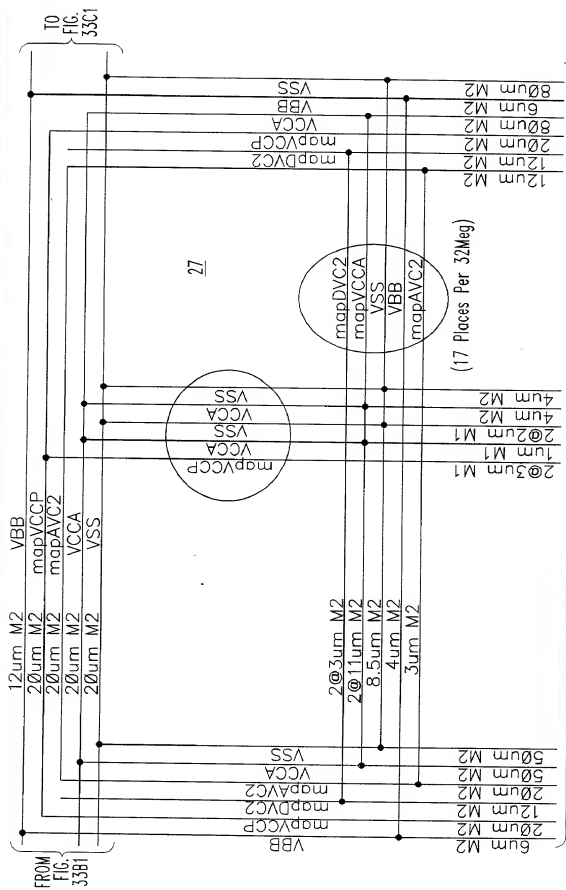


FIG. 33A4



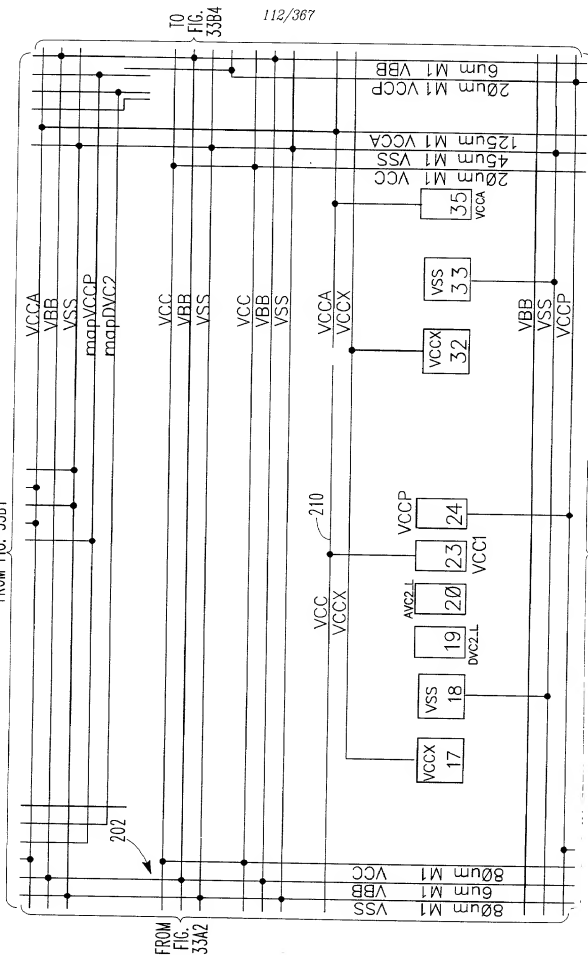
FIG. 33B1



TO FIG. 33B4

FIG. 33B2

FROM FIG. 33B1



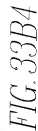
FROM
FIG.
33A2

TO
FIG.
33B4

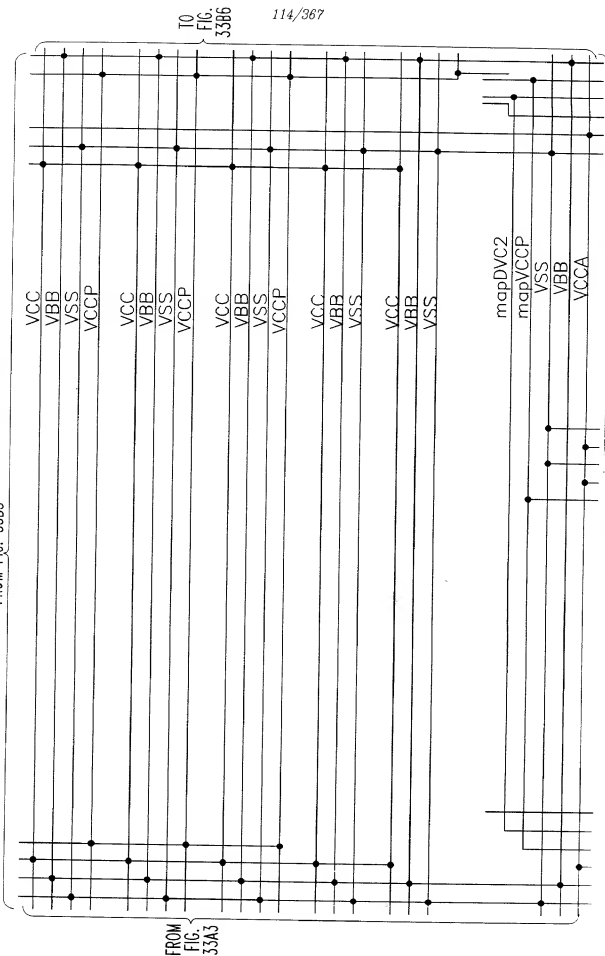
112/367

TO FIG. 33B3

FIG. 33B3



FROM FIG. 33B3

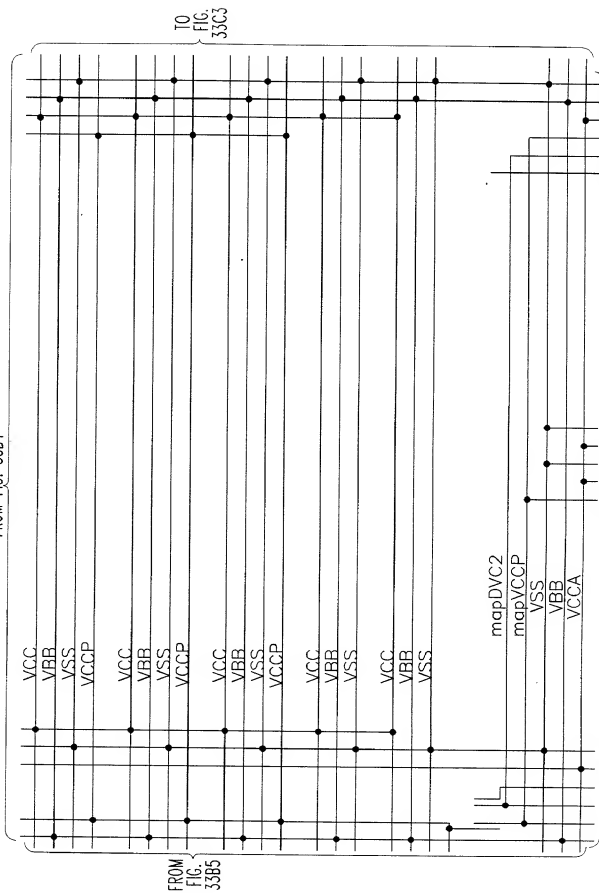


TO FIG. 33B7

FIG. 33B5

T080200 02910860

FROM FIG. 33B4



TO FIG. 33B8

FIG. 33B6

38

(17 Places Per 32Meg)

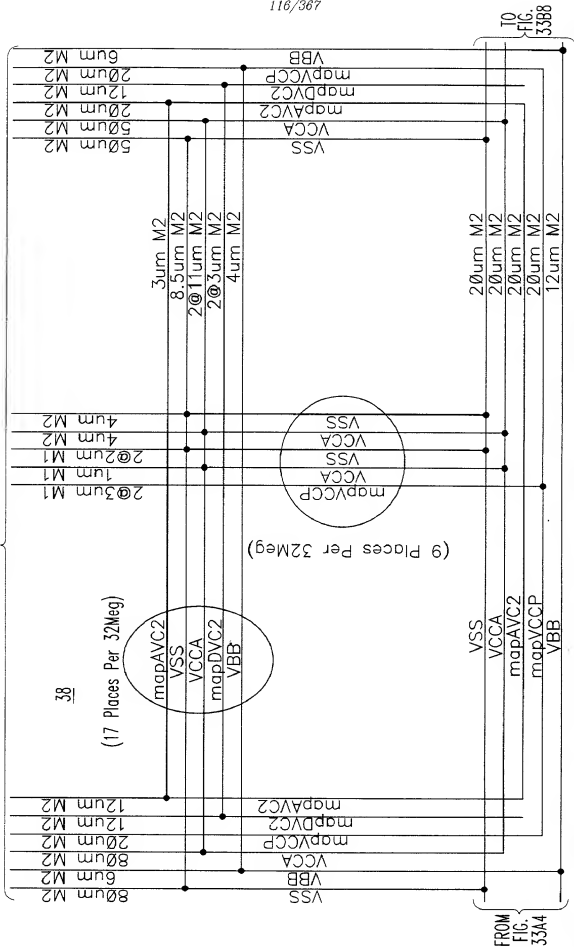


FIG. 33B7

FROM FIG. 33B6

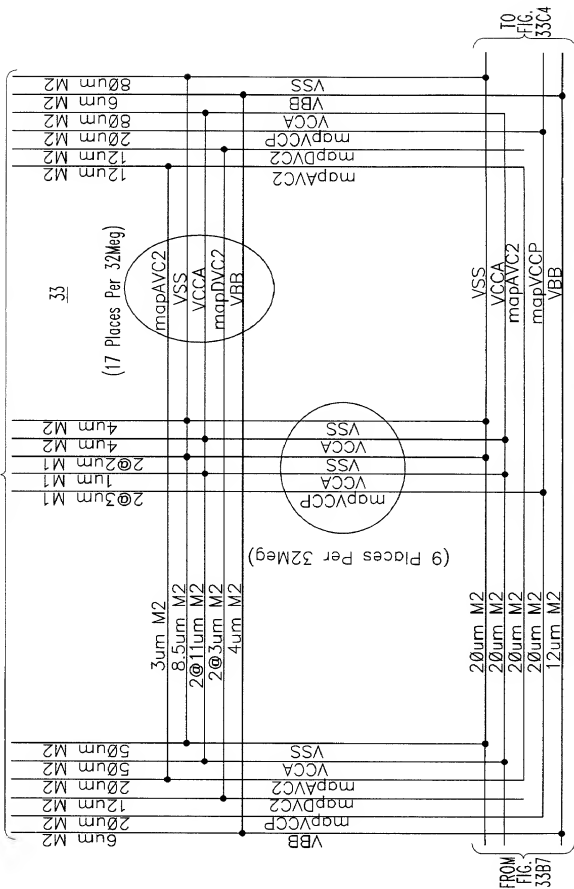
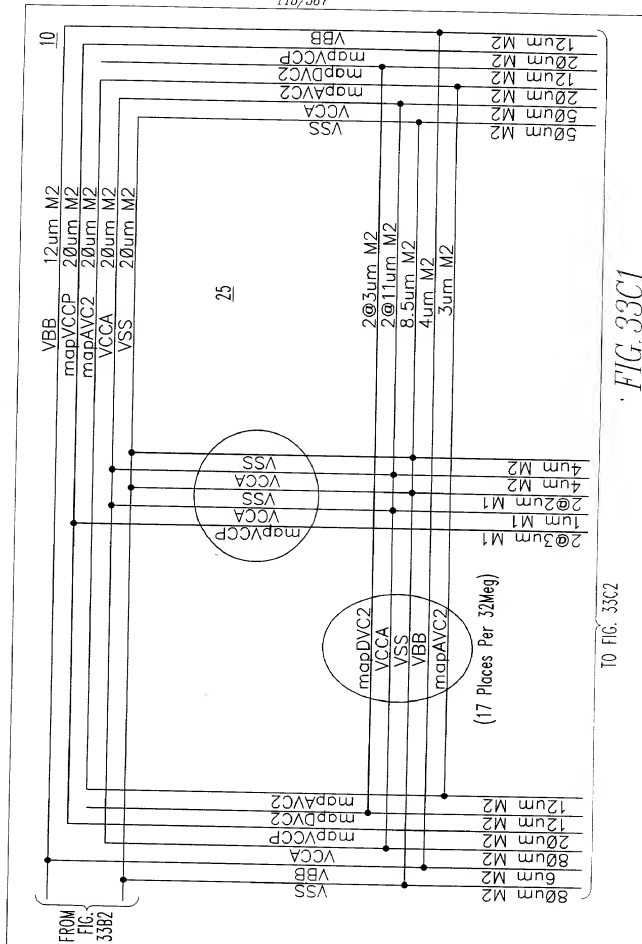
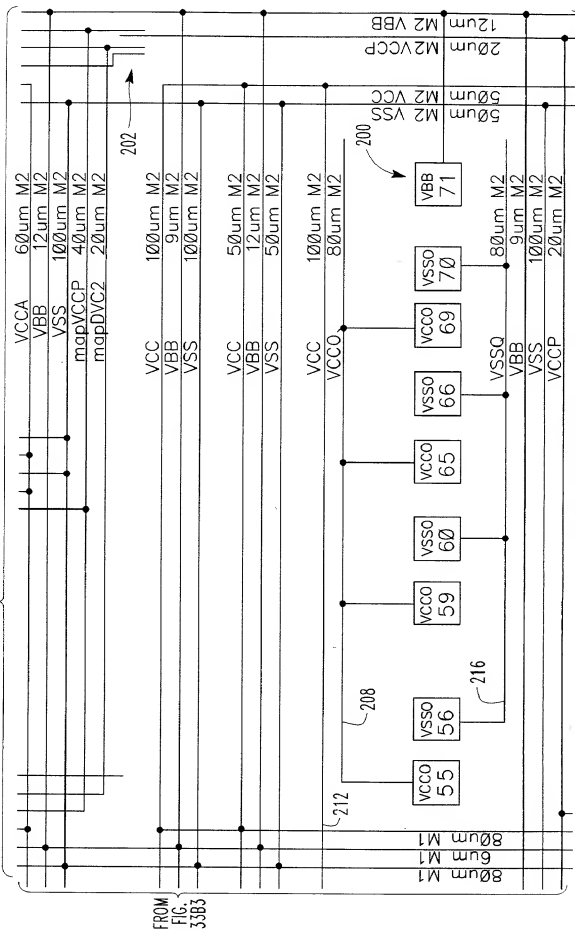


FIG. 33B8



TO FIG. 33C2

FROM FIG. 33C1



TO FIG. 33C3

FIG. 33C2

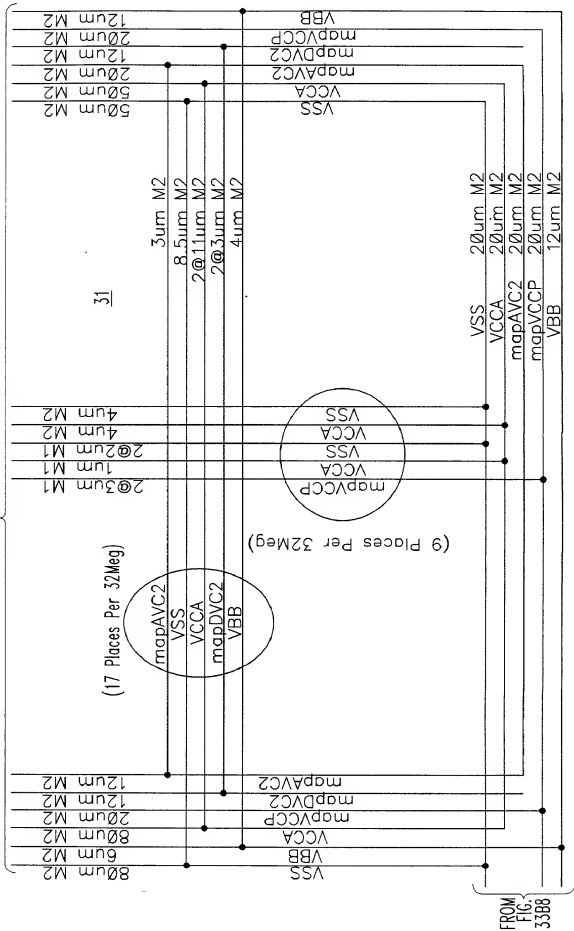
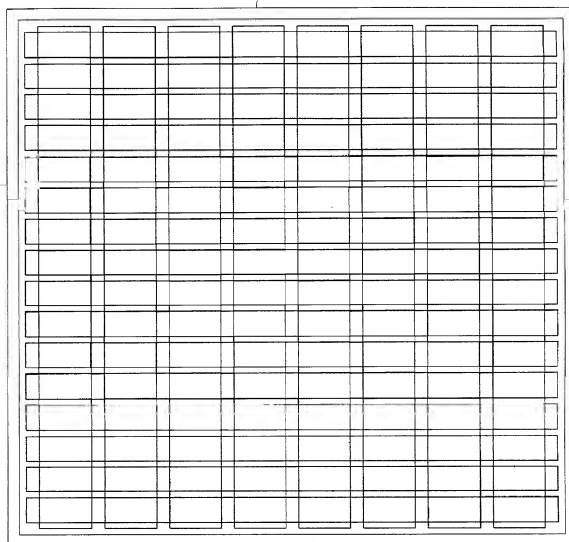


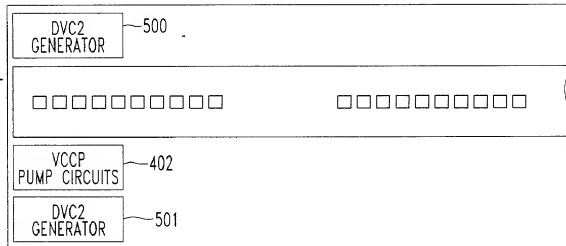
FIG. 33C4

10

45



200

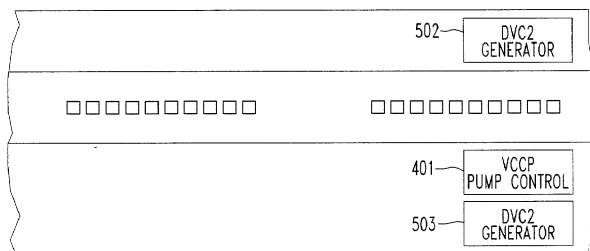
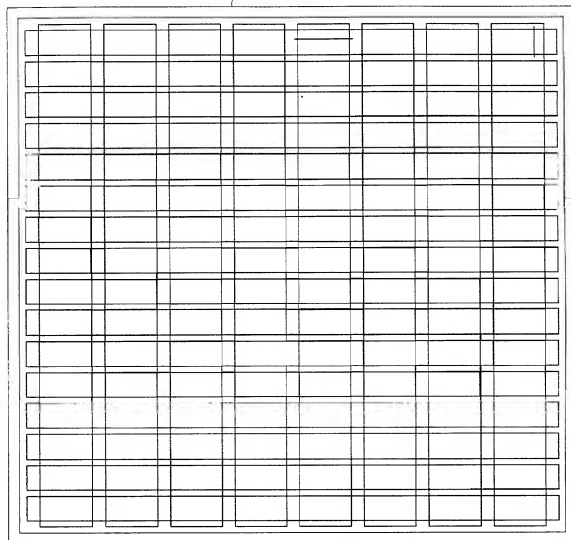
TO
FIG. 33D3

TO FIG. 33D2

FIG. 33D1

TO FIG. 33D1

47

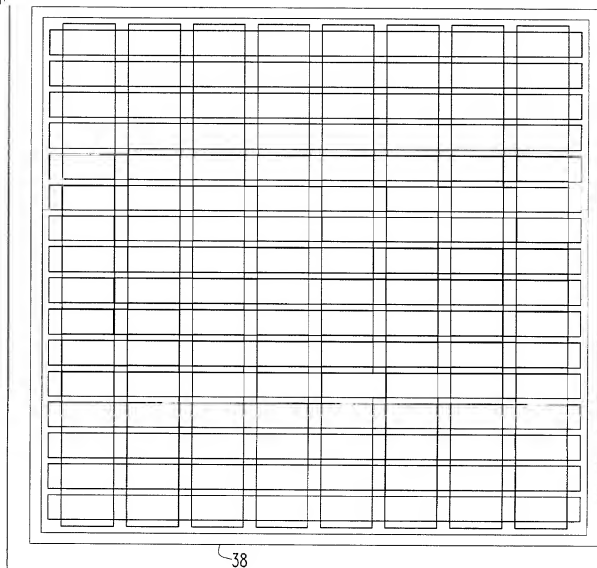


TO
FIG.
33D4

FIG. 33D2

TO
FIG.
33D1

(SEE FIG. 33E1)



TO FIG. 33D4

FIG. 33D3

(SEE FIG. 33D2)

25

TO FIG. 33E2

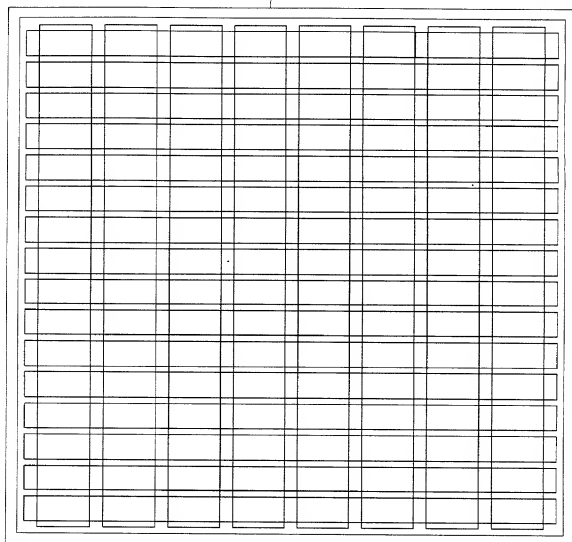
DVC2
GENERATOR 504VCCP
REGULATOR 220DVC2
GENERATOR 505TO
FIG.
33E3

FIG. 33E1

-10

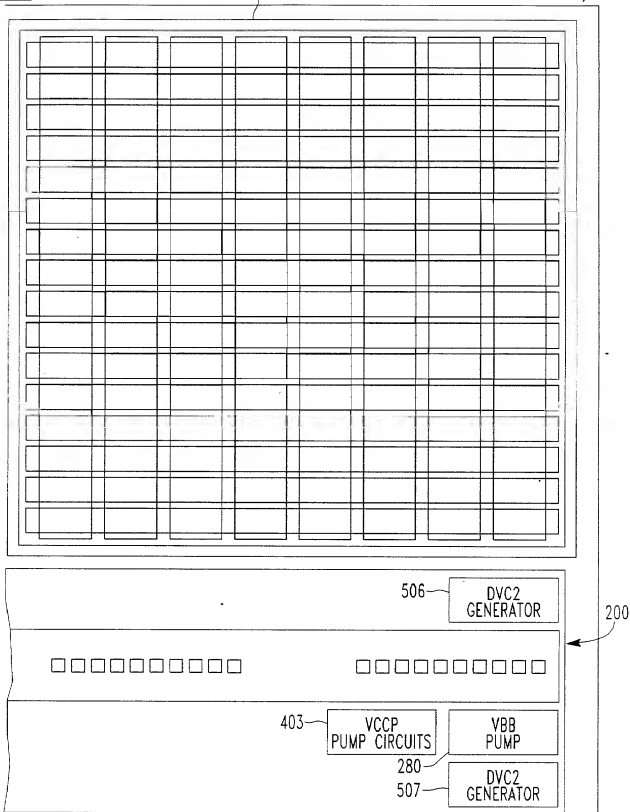


FIG. 33E2

TO
FIG.
33E4

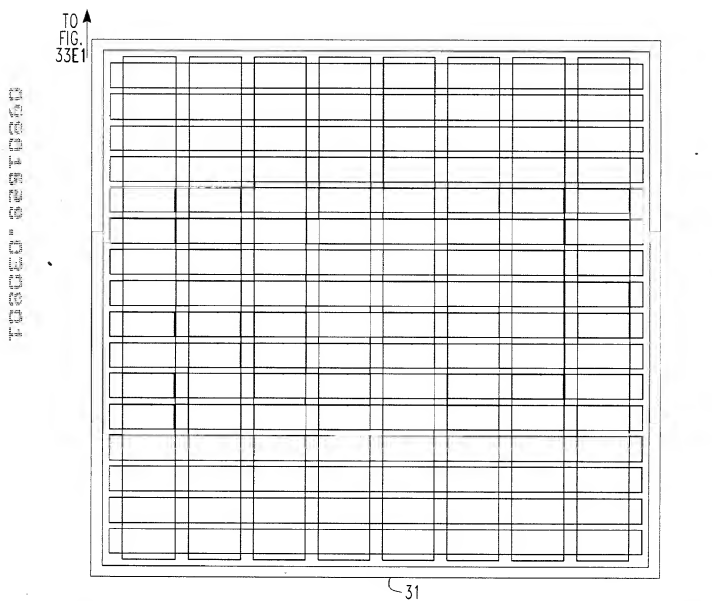


FIG. 33E3

00001520 020004

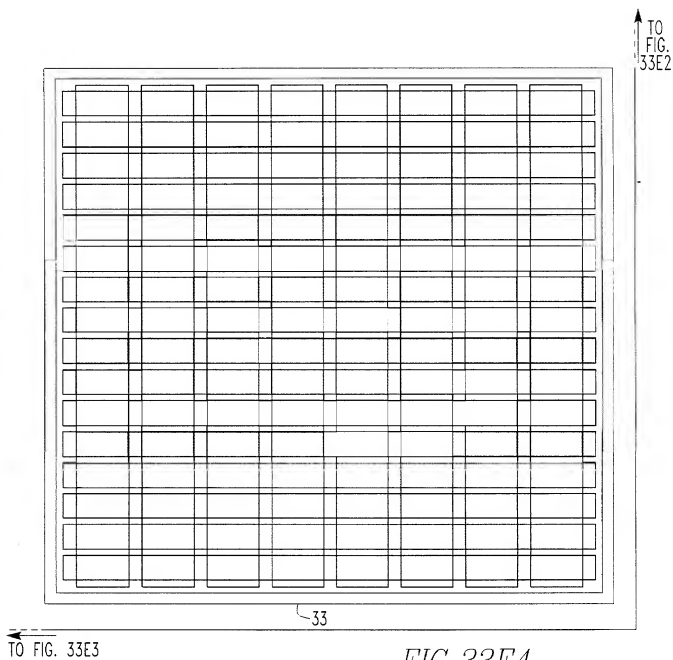
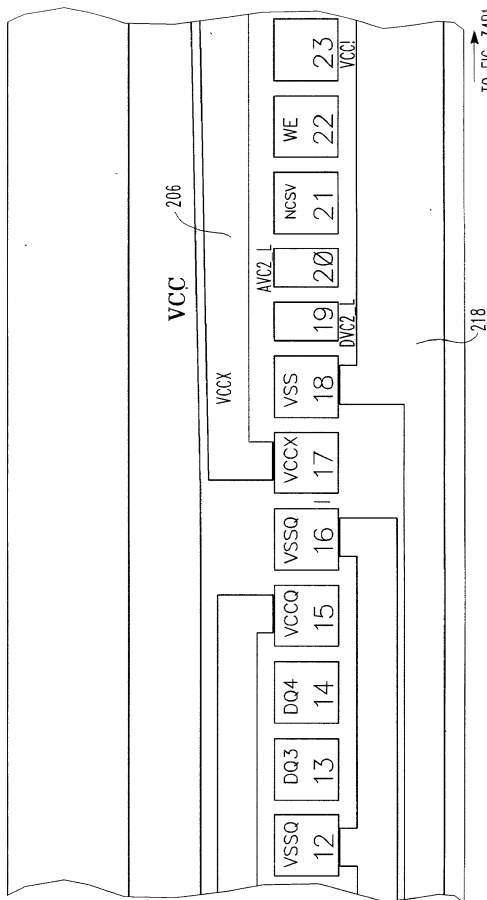


FIG. 33E4

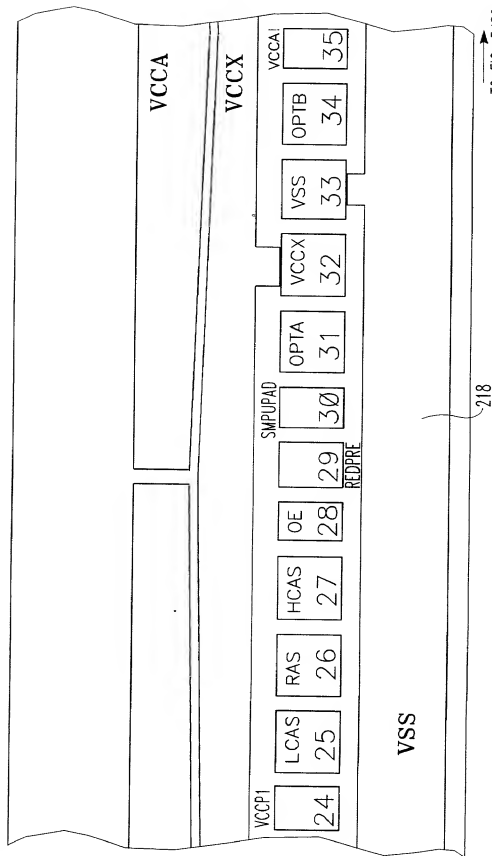
TO FIG. 34A1
←



TO FIG. 34B1
→

FIG. 34A2

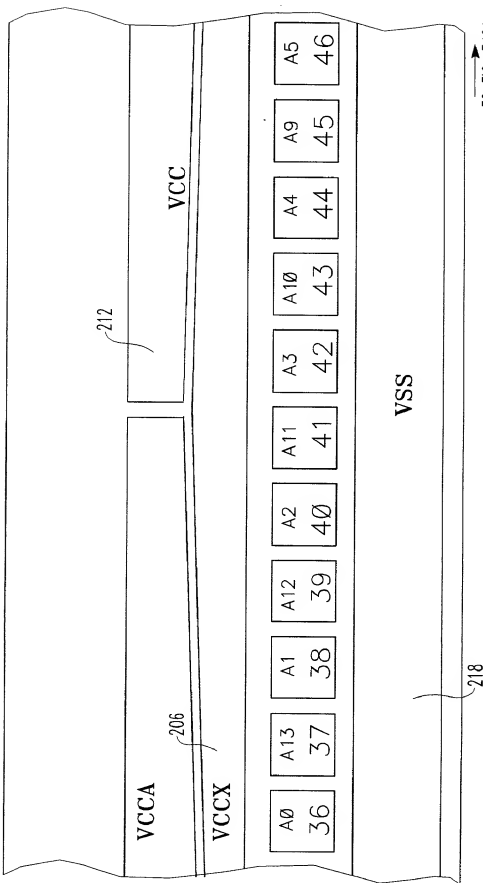
TO FIG. 34A2



TO FIG. 34B2

FIG. 34B1

TO FIG. 34B1



TO FIG. 34C1

FIG. 34B2

TO FIG. 34B2

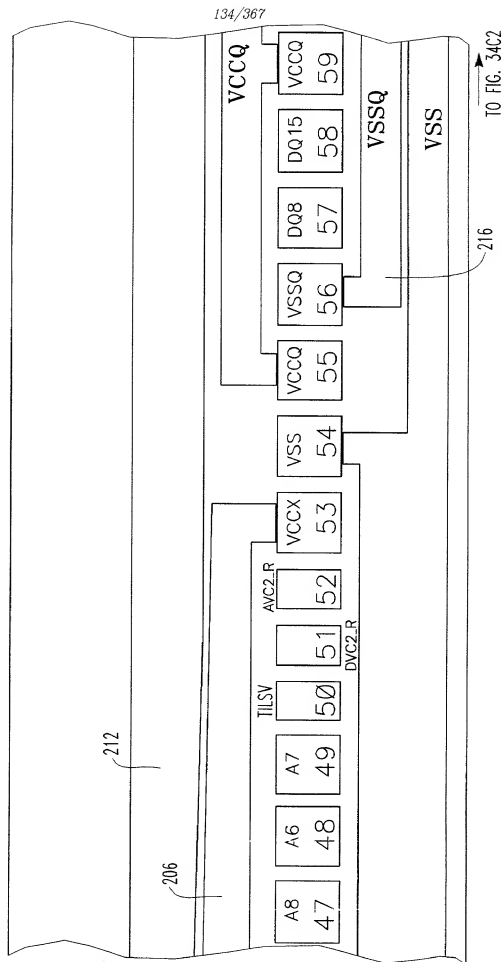


FIG. 34C1

TO FIG. 34C1

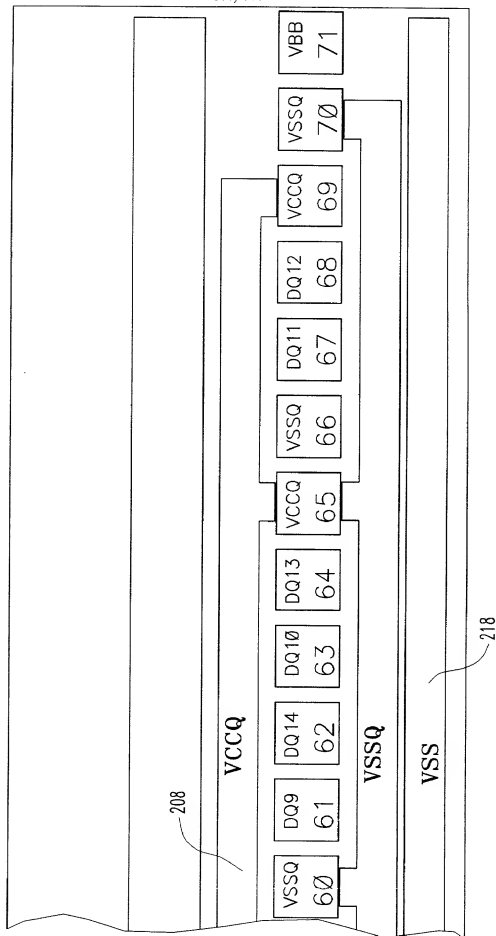


FIG. 34C2

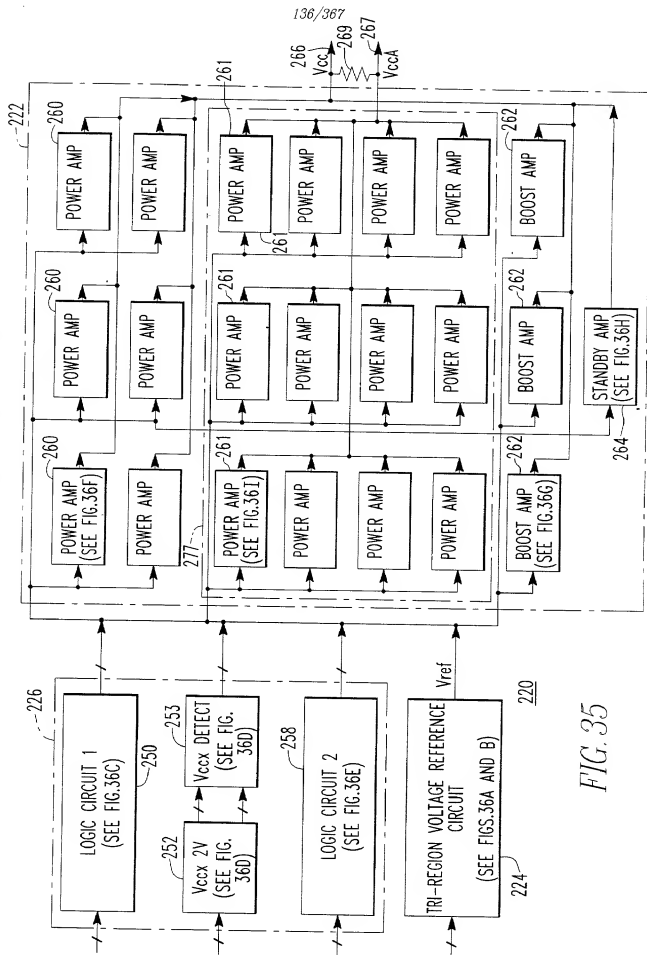


FIG. 35



FIG. 36A1

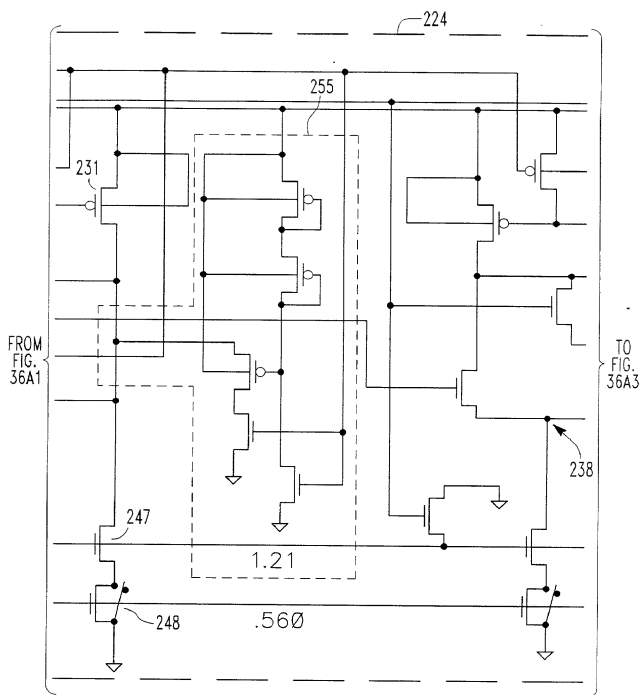


FIG. 36A2

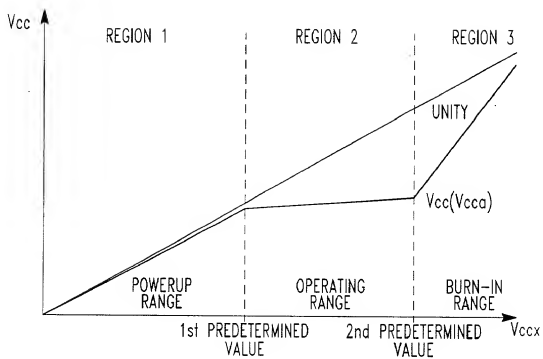


FIG. 36B

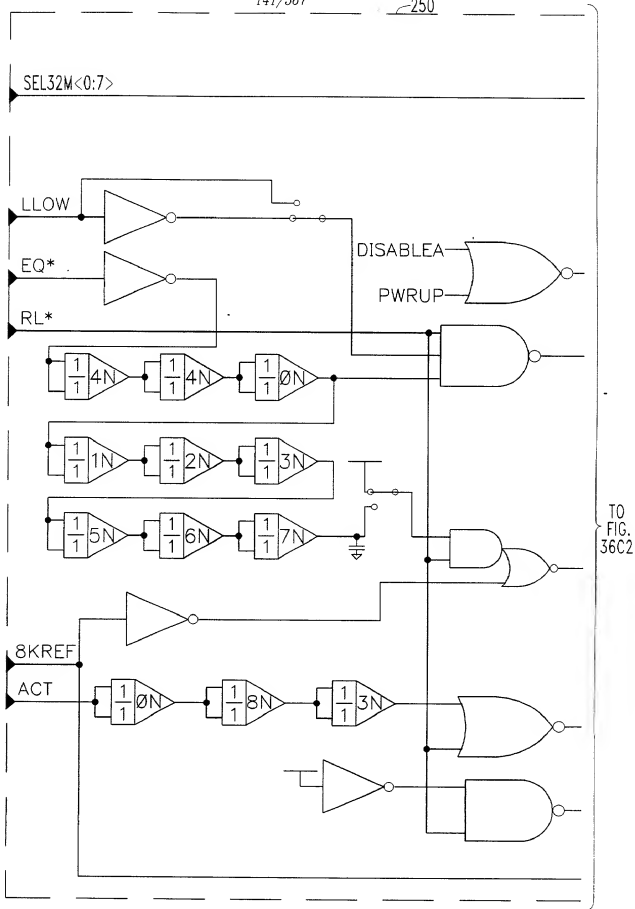


FIG. 36C1

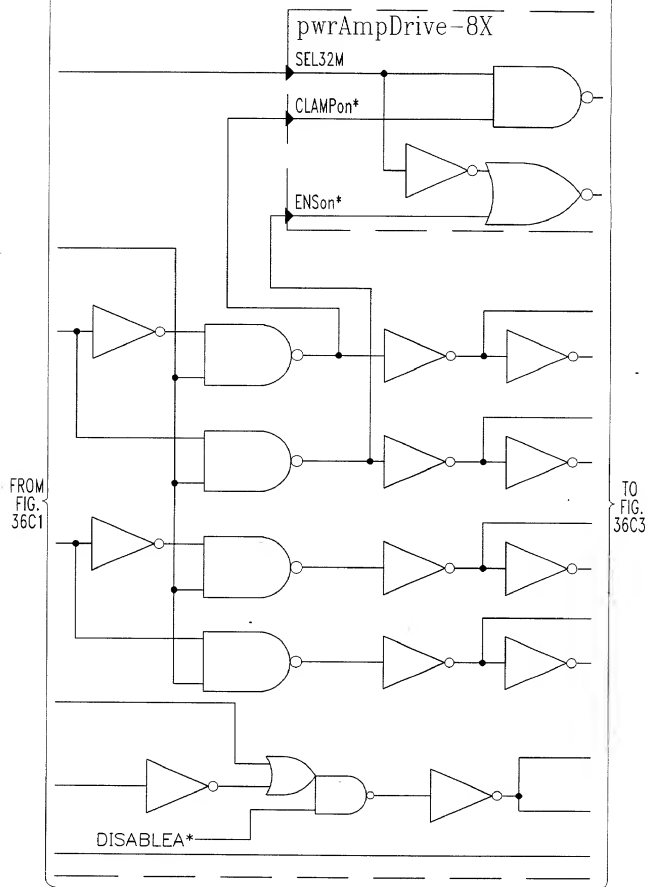


FIG. 36C2

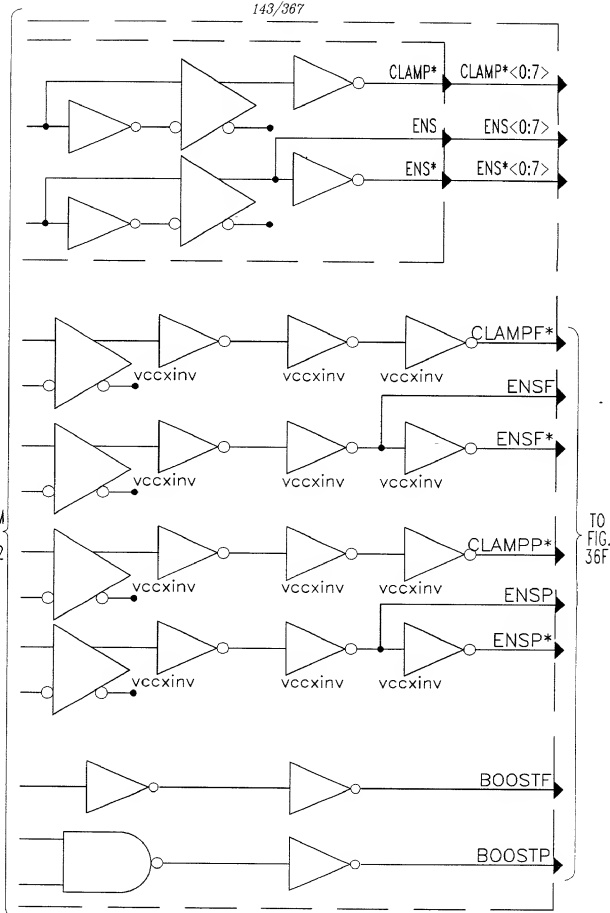
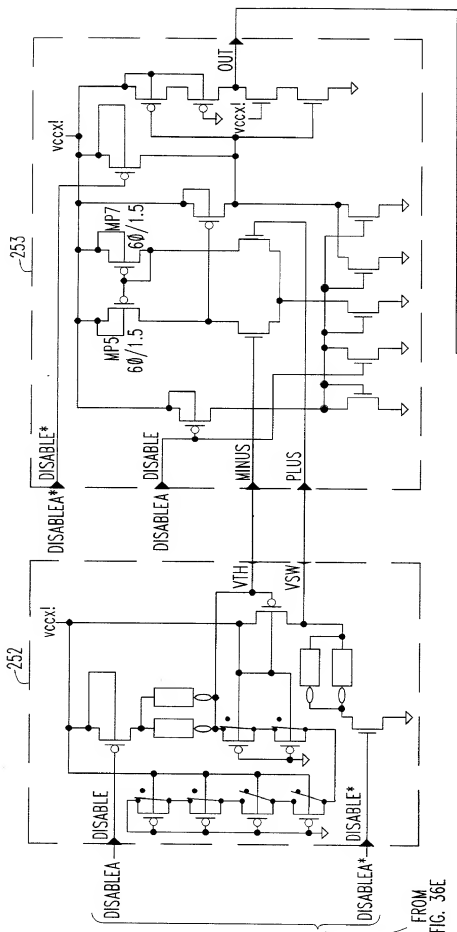


FIG. 36C3



FROM
FIG. 36E

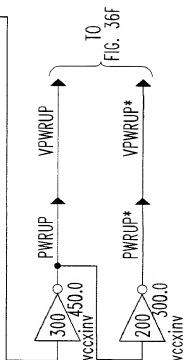
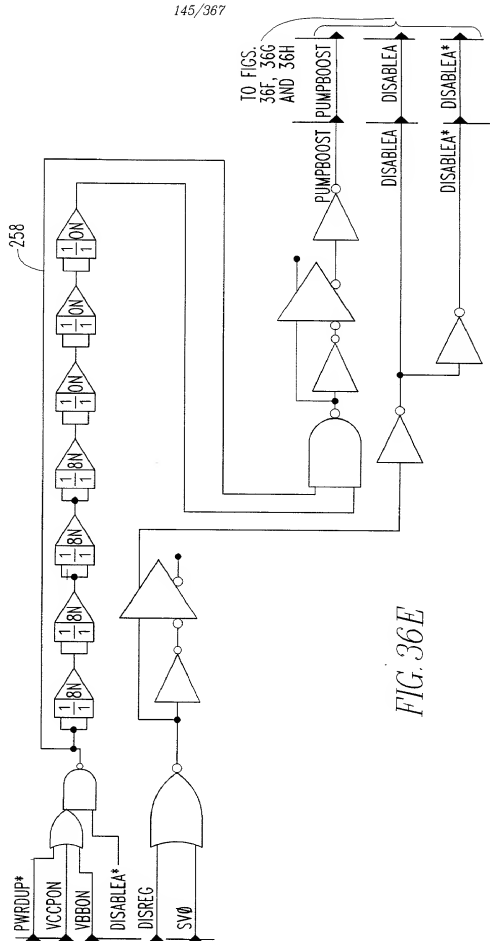
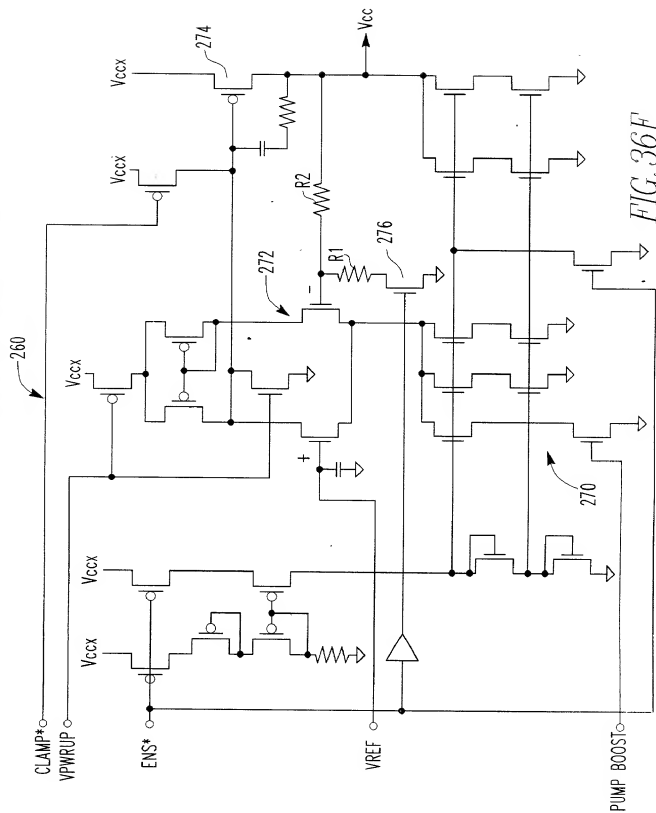
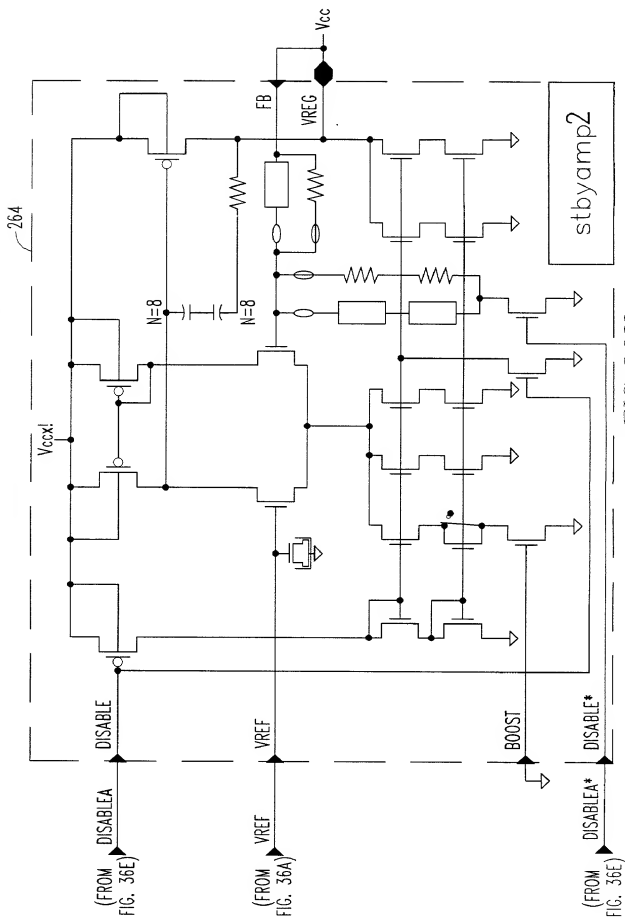
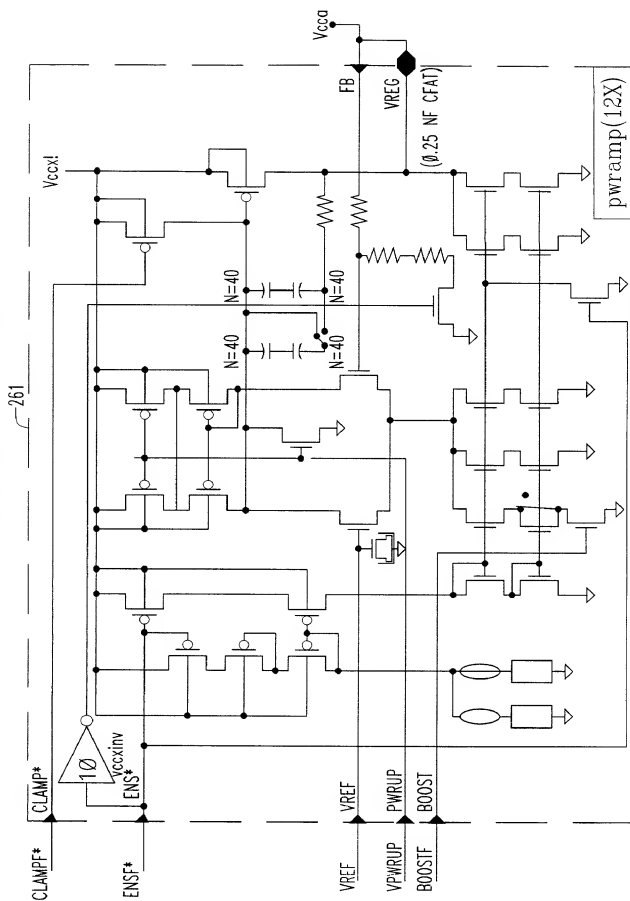


FIG. 36D









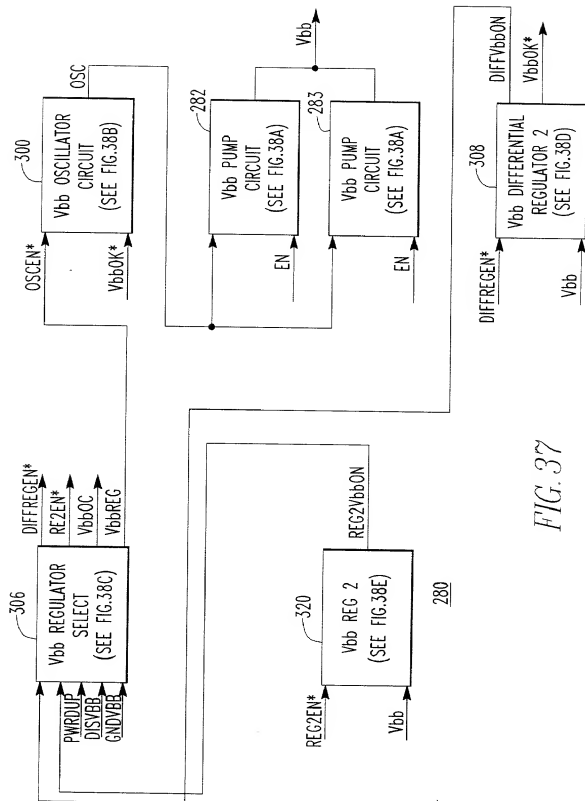
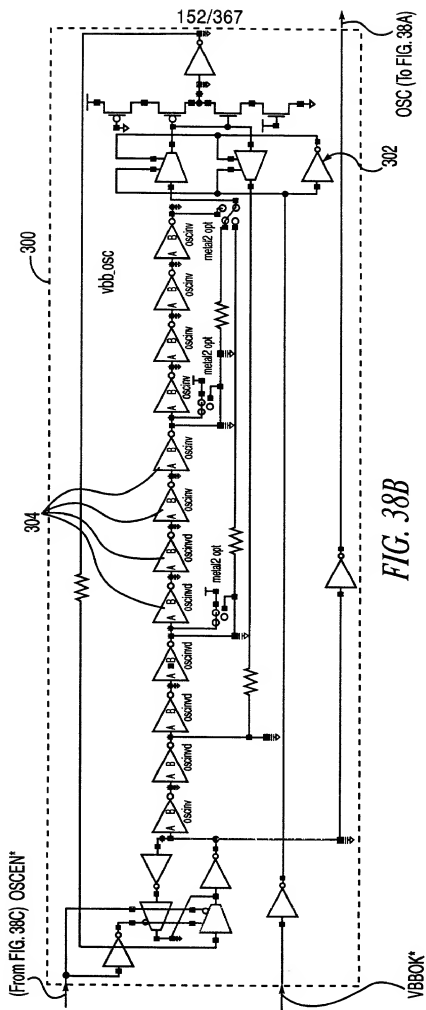


FIG. 37



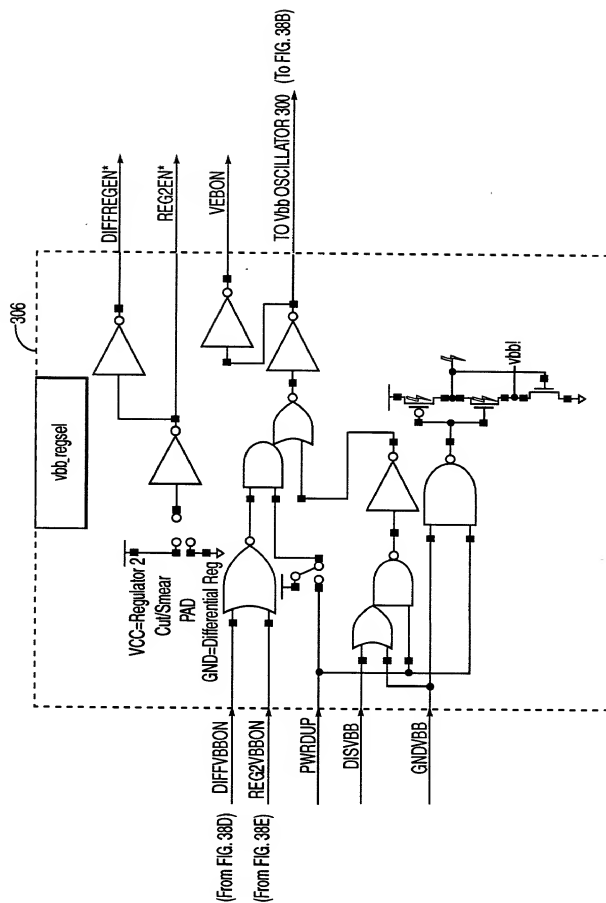


FIG. 38C

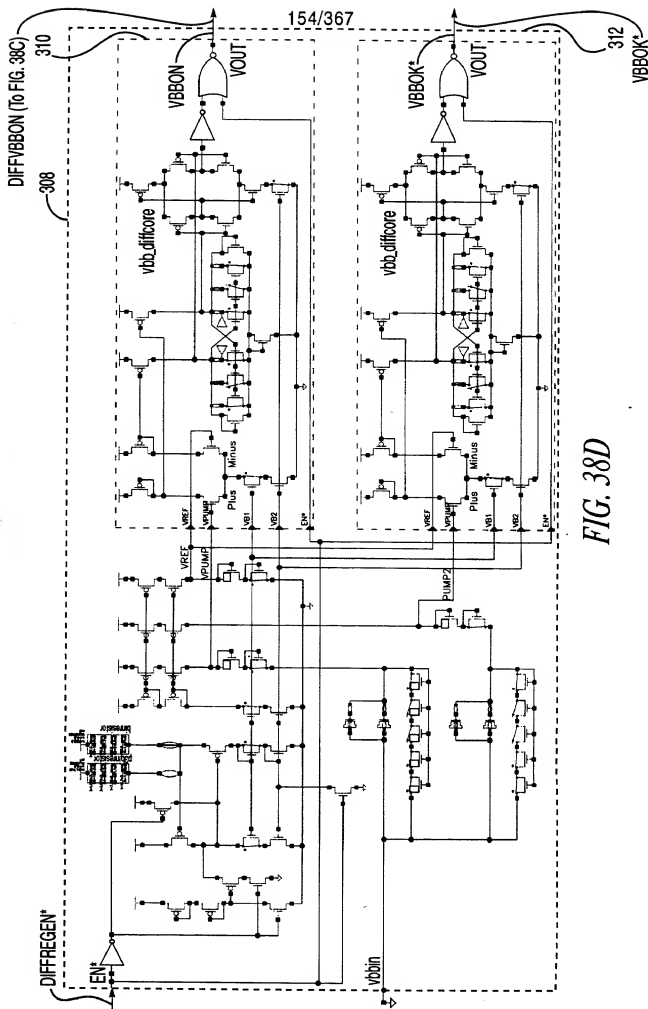


FIG. 38D

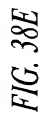


FIG. 38E

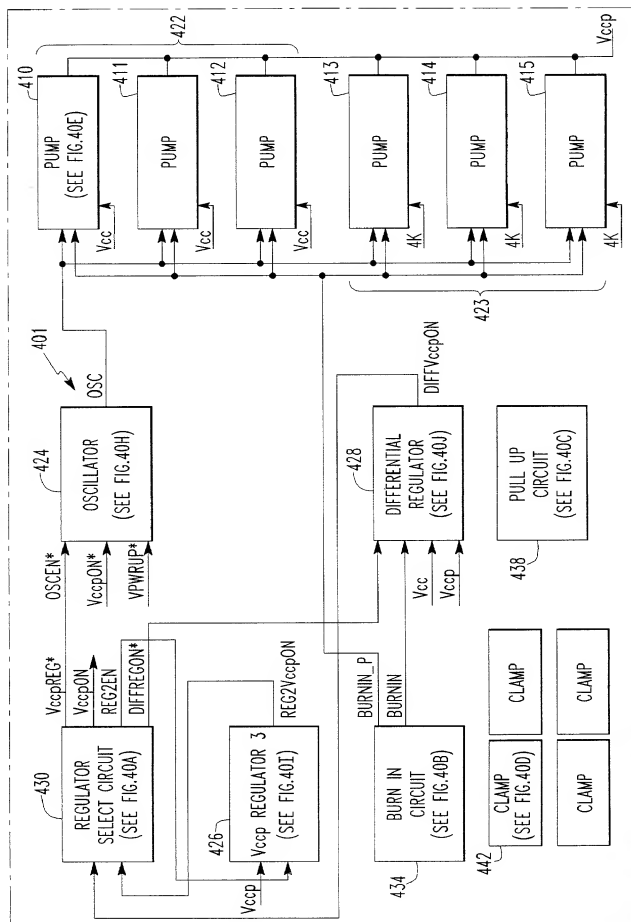


FIG. 39

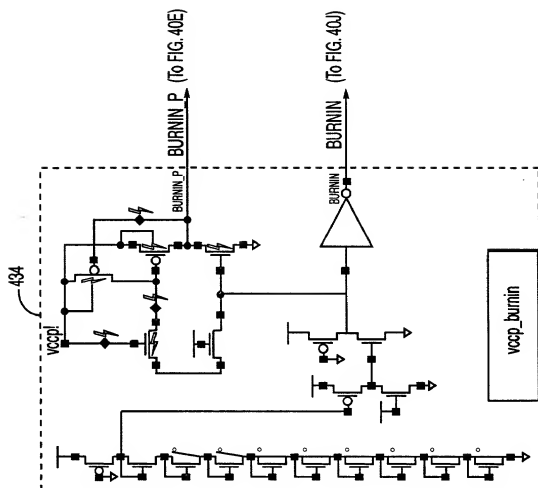
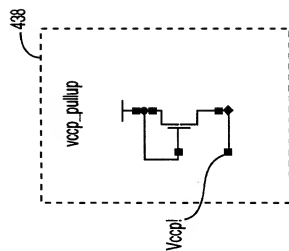


FIG. 40B

*FIG. 40C*

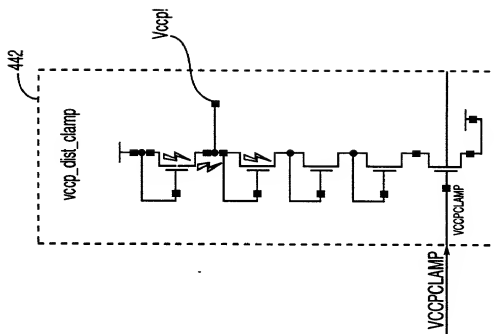
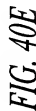


FIG. 40D



(From FIG. 40B) BURNIN P
(From FIG. 40H) VCCPOSC

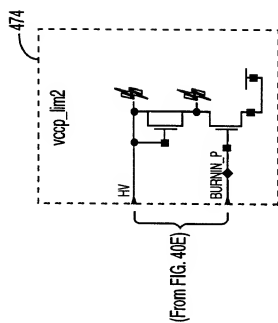


FIG. 40F

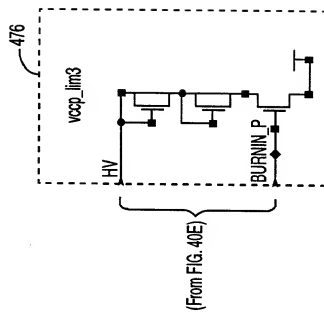
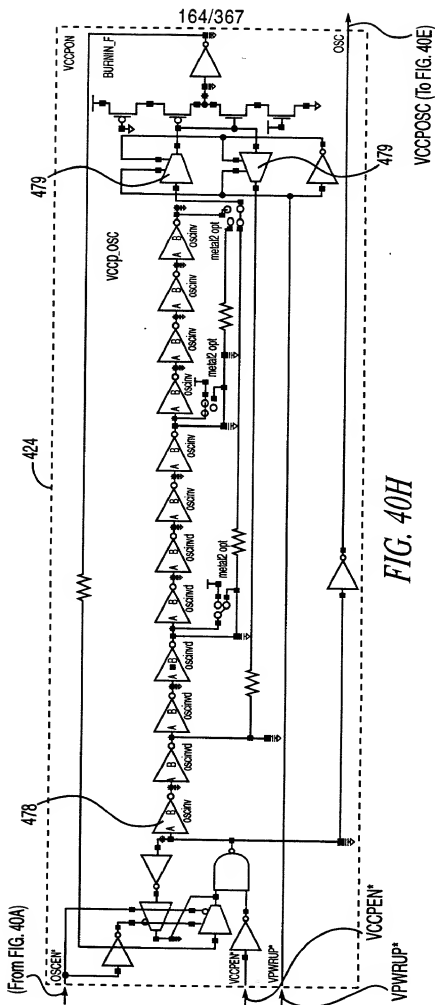


FIG. 40G



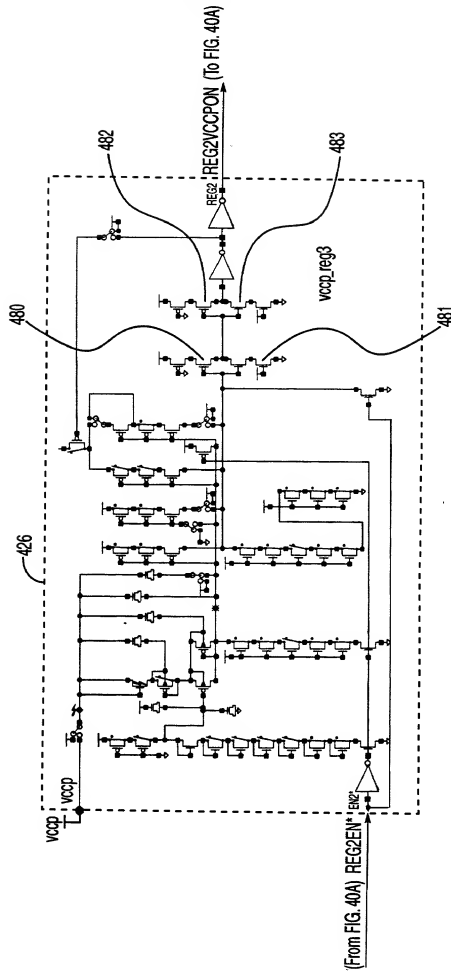


FIG. 40I

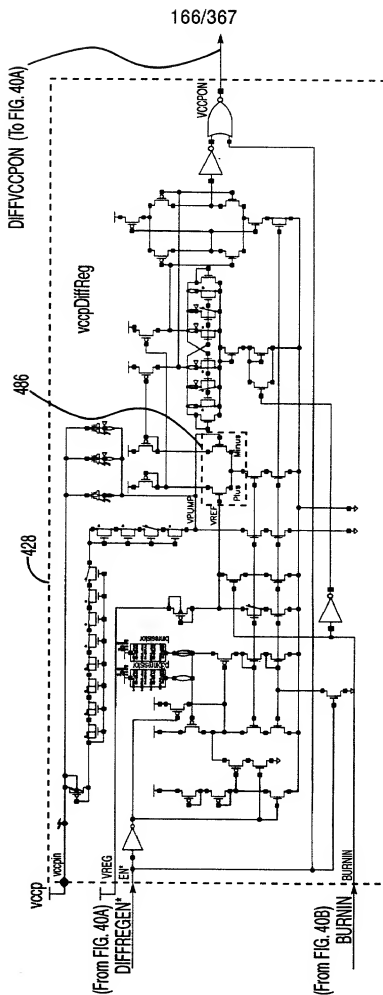


FIG. 40J

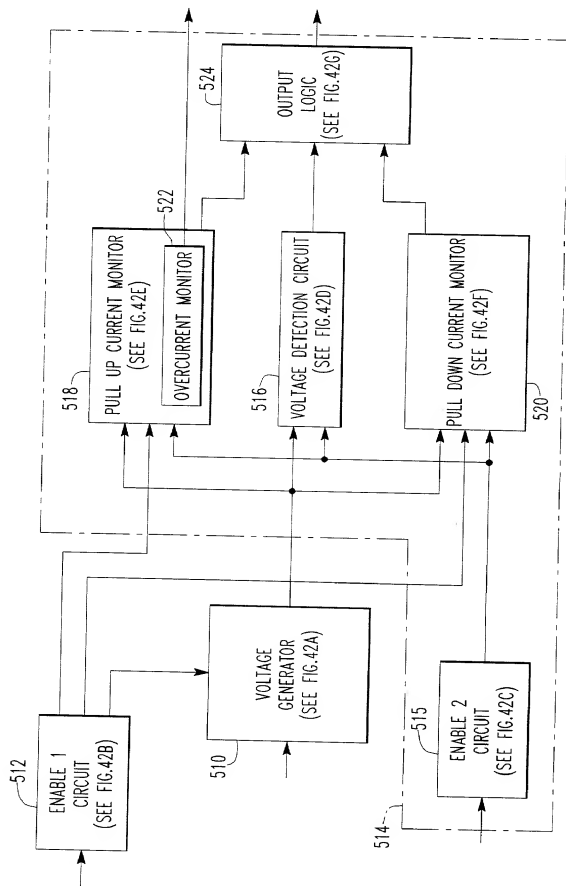


FIG. 41

500

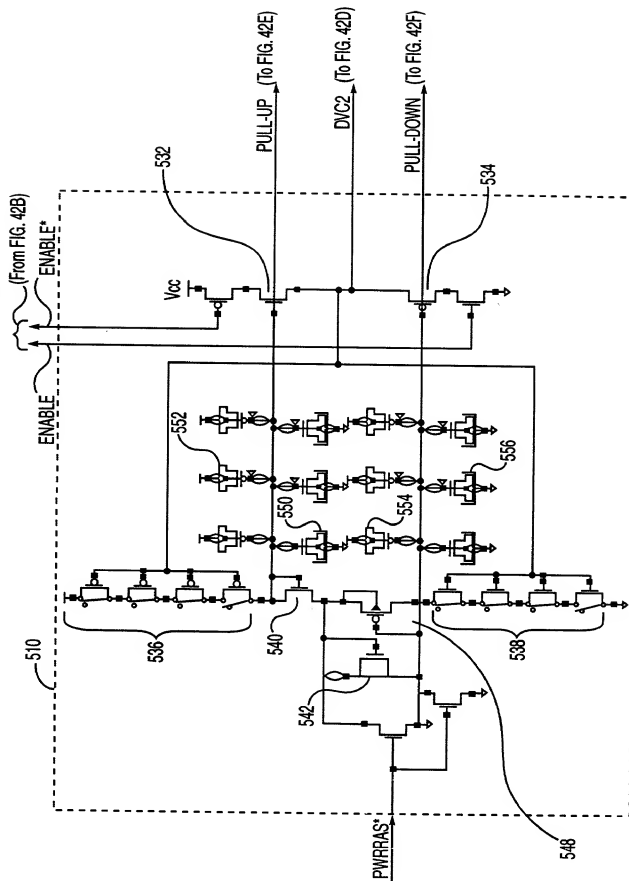


FIG. 42A

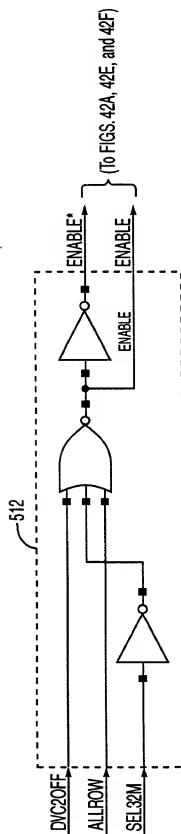


FIG. 42B

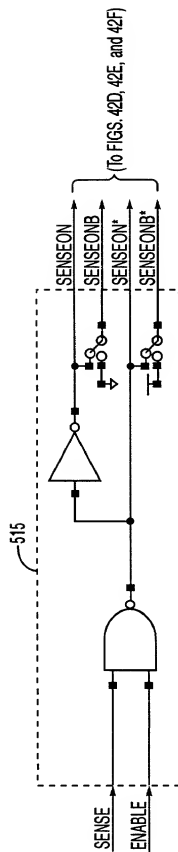


FIG. 42C

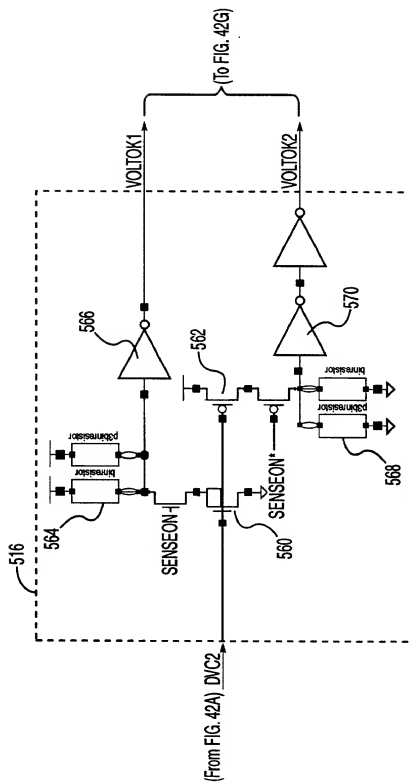


FIG. 42D

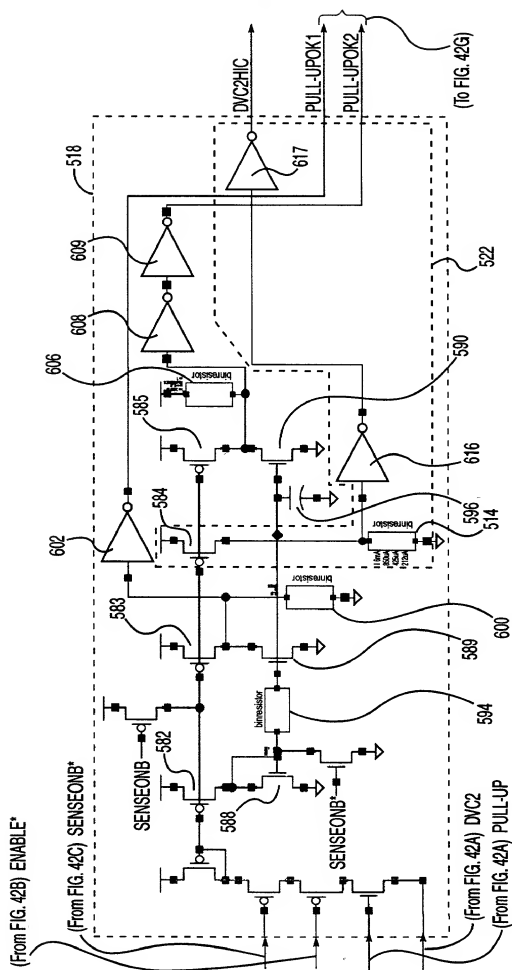


FIG. 42E

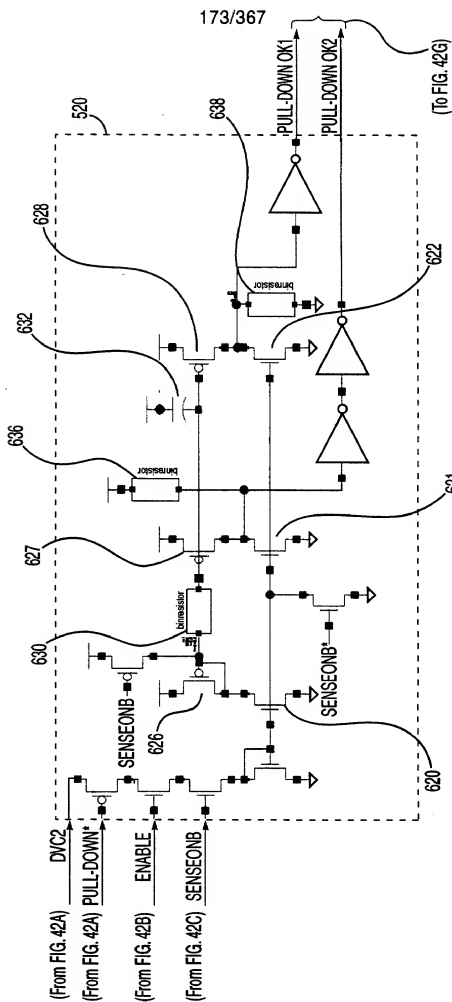


FIG. 42F

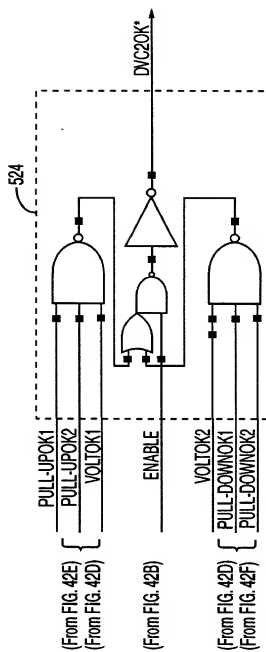


FIG. 42G



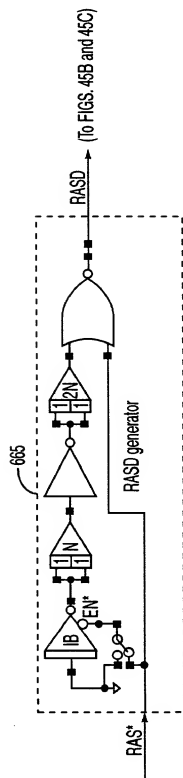
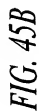


FIG. 45A



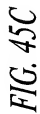


FIG. 45C

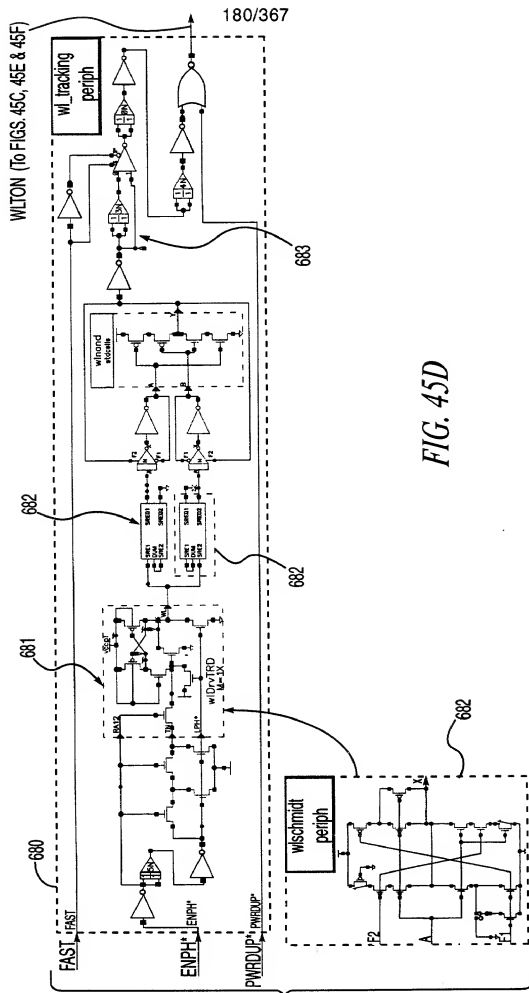


FIG. 45D

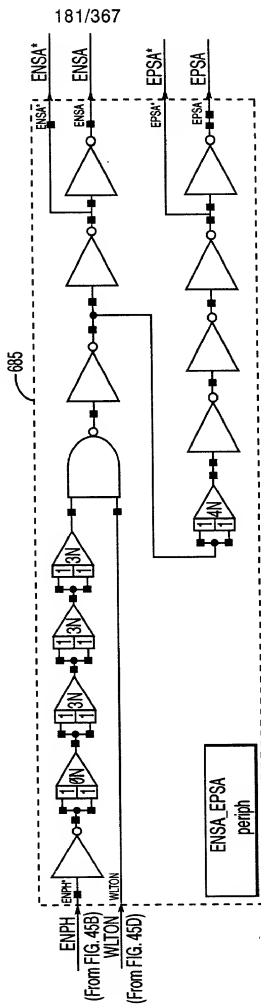


FIG. 45E

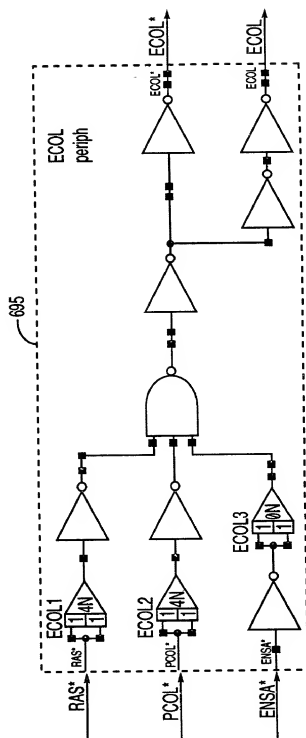


FIG. 45G

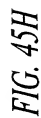


FIG. 45H



FIG. 45I

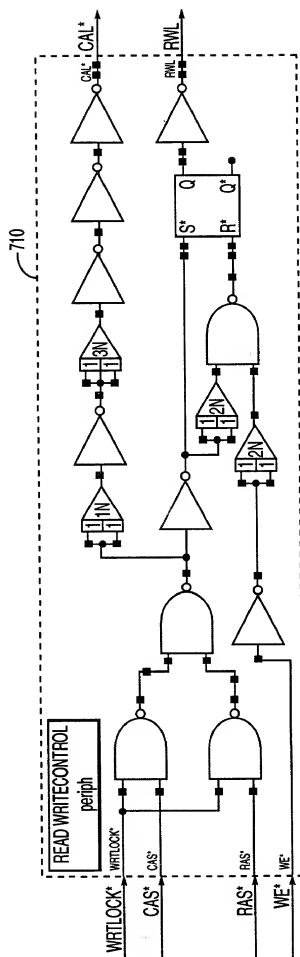


FIG. 45J

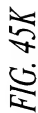


FIG. 45K

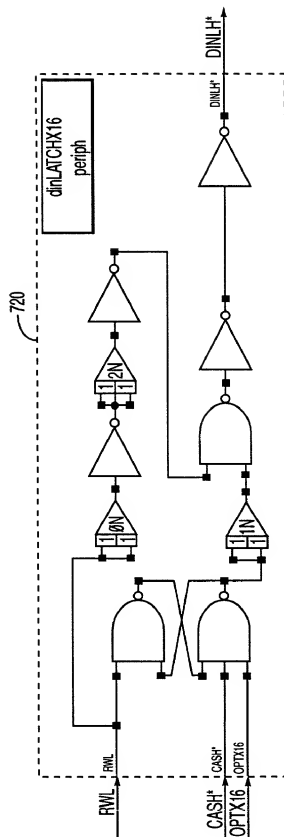


FIG. 45L

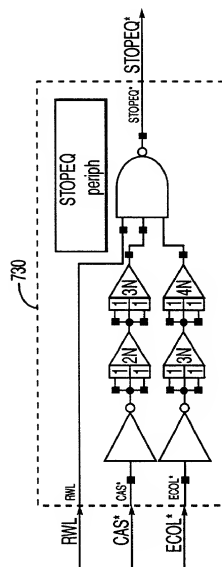


FIG. 45N

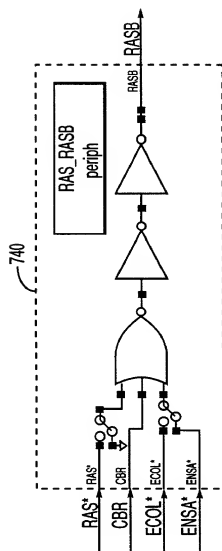


FIG. 45P

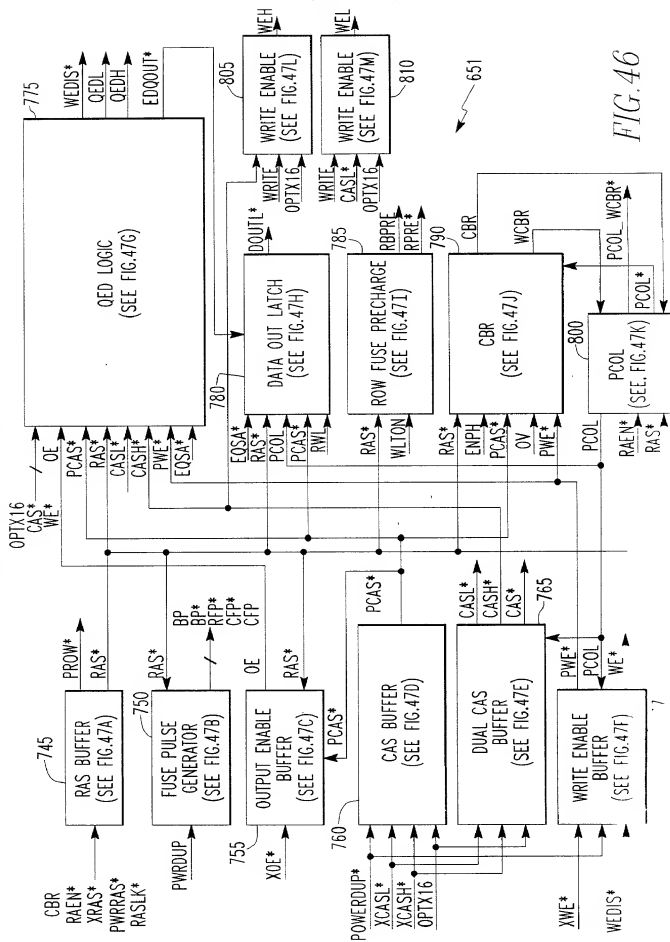


FIG. 46

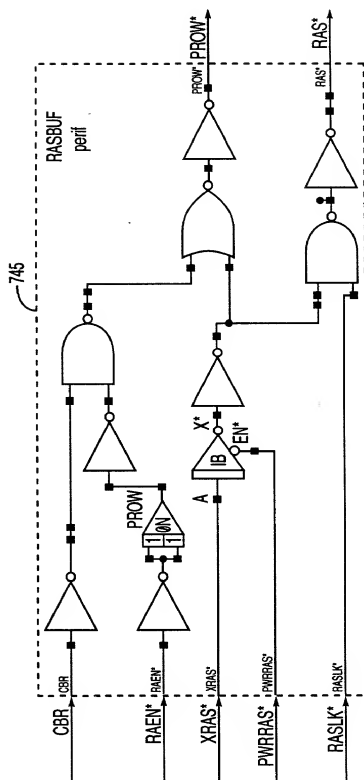


FIG. 47A

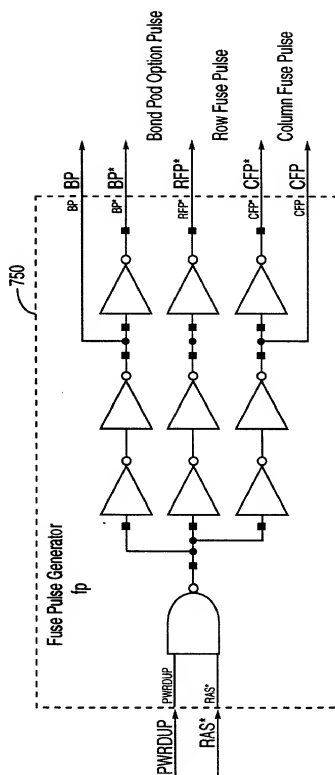


FIG. 47B

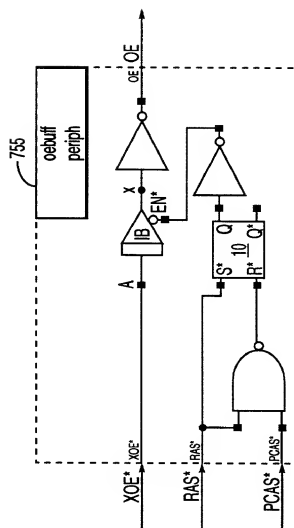


FIG. 47C

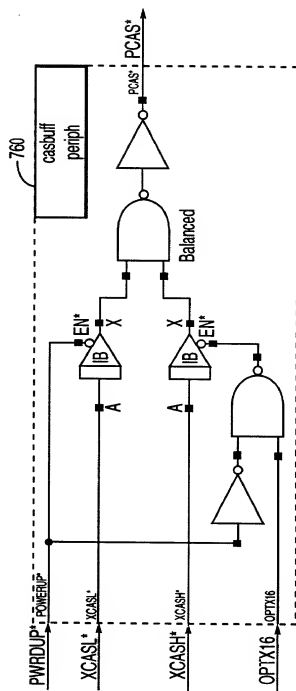


FIG. 47D

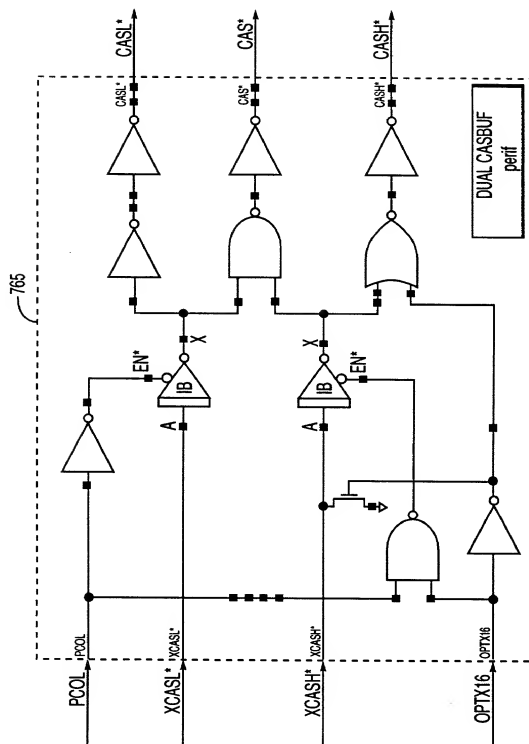


FIG. 47E

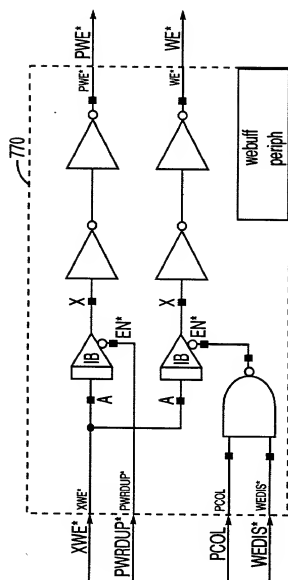


FIG. 47F

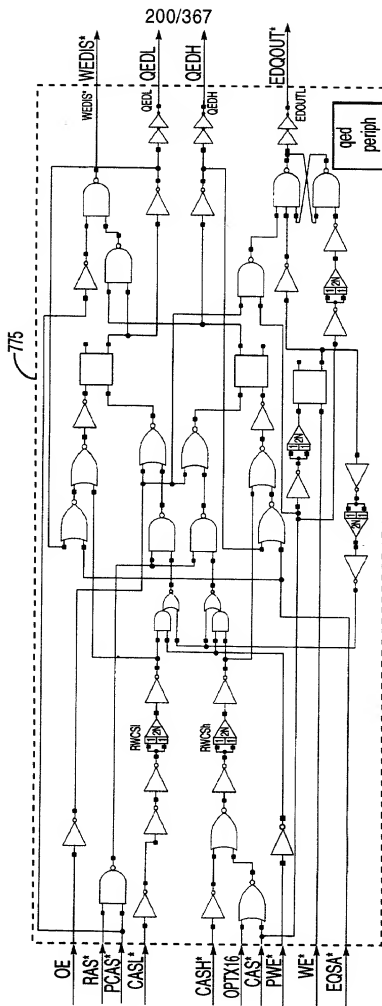


FIG. 47G

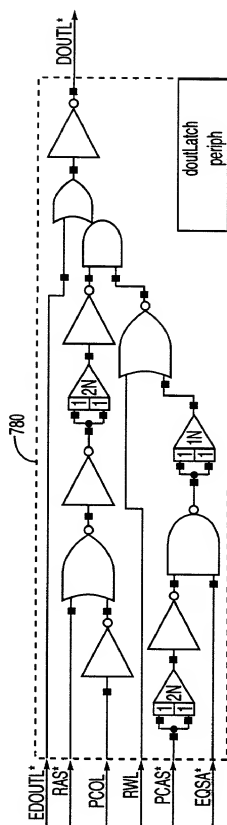


FIG. 47H

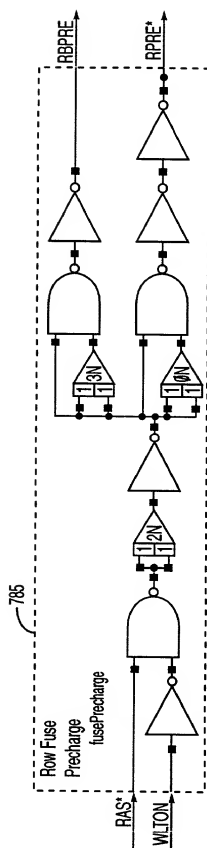


FIG. 471

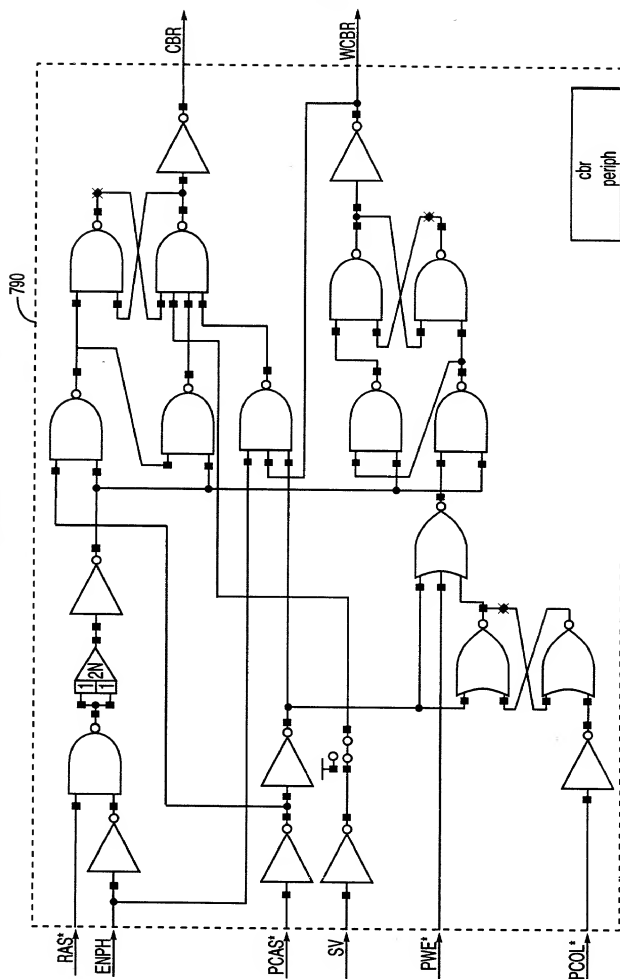


FIG. 47J

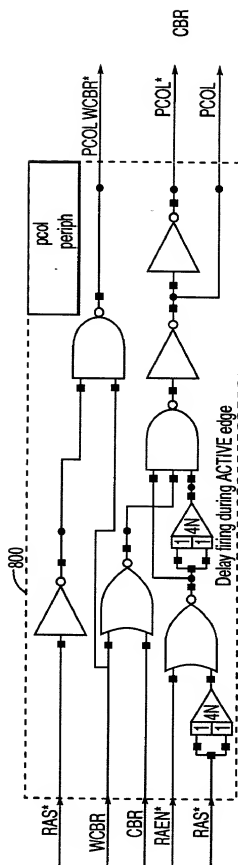


FIG. 47K

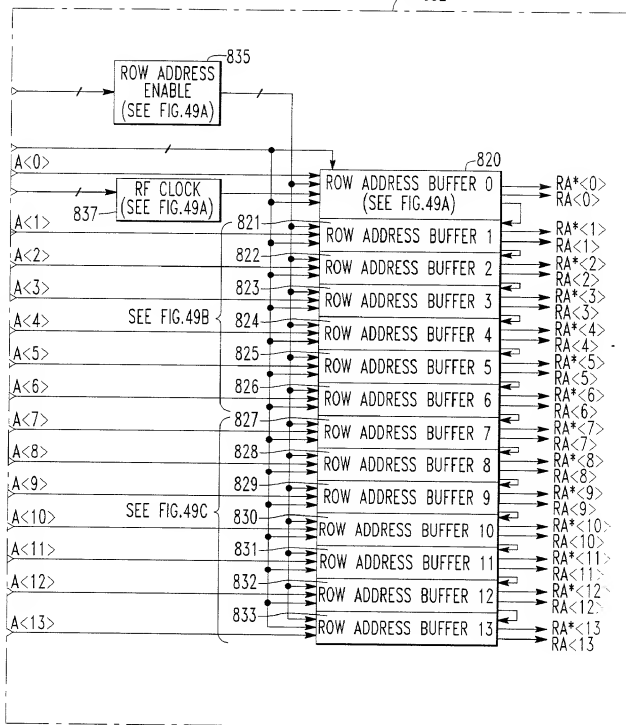


FIG. 48A

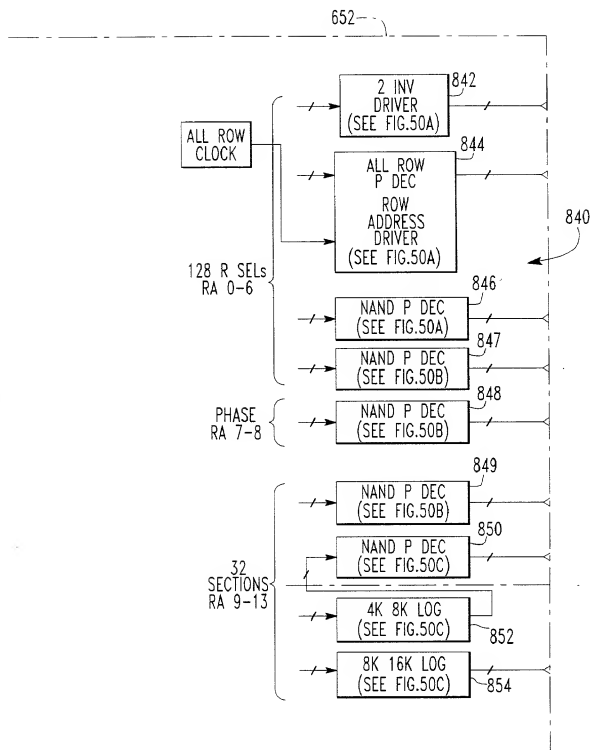
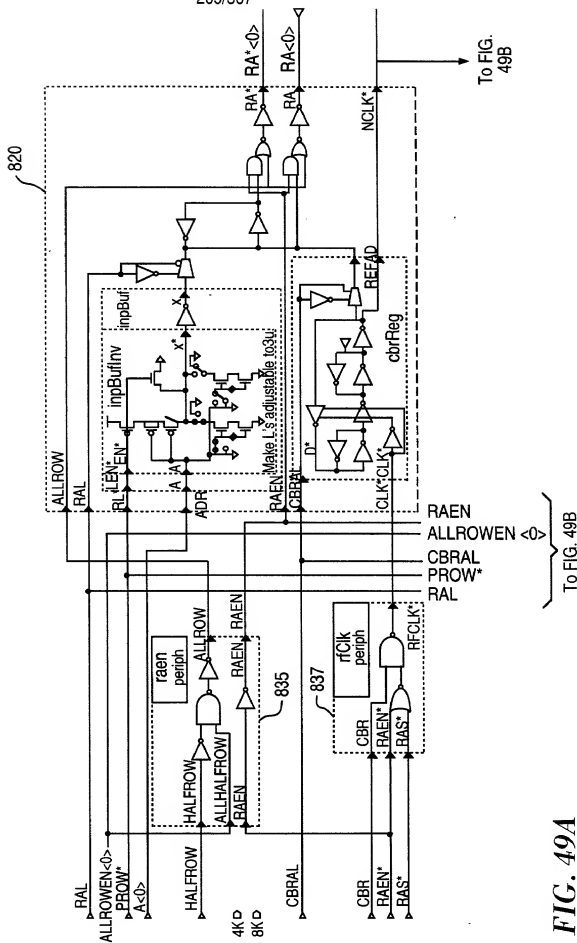


FIG. 48B

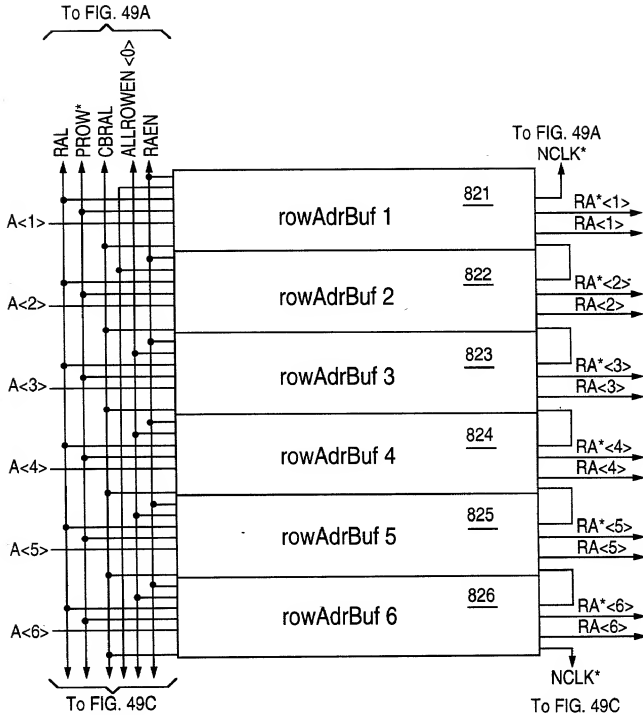
209/367



To FIG.
49B

FIG. 49A

To FIG. 49B

**FIG. 49B**

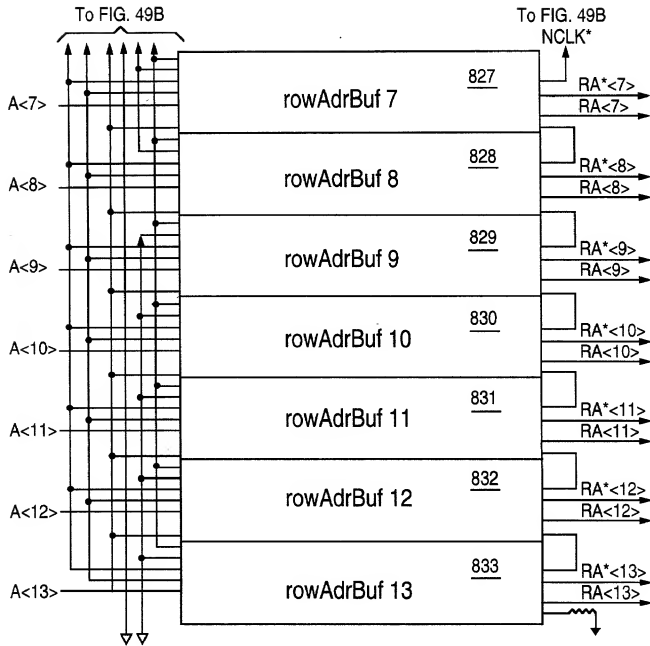


FIG. 49C

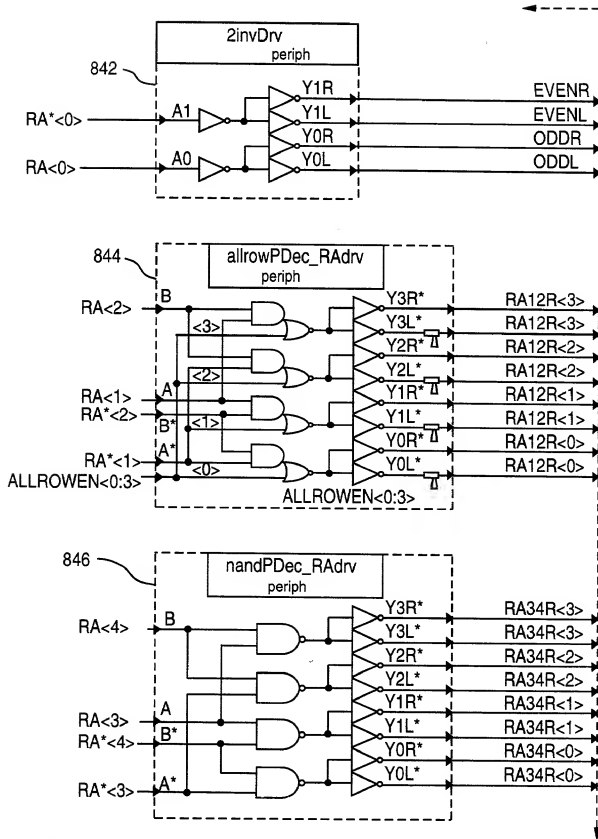


FIG. 50A

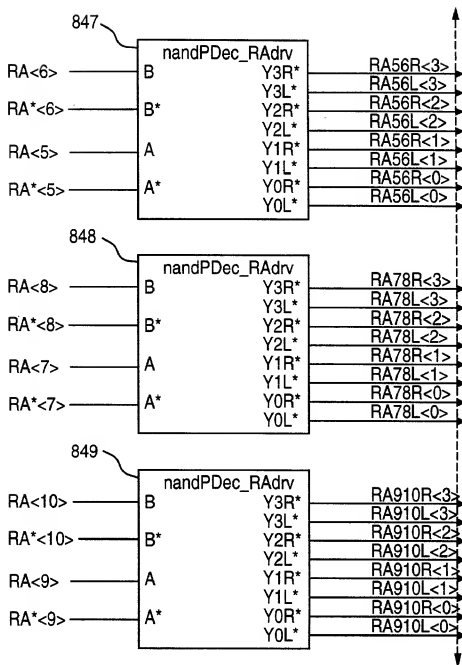


FIG. 50B

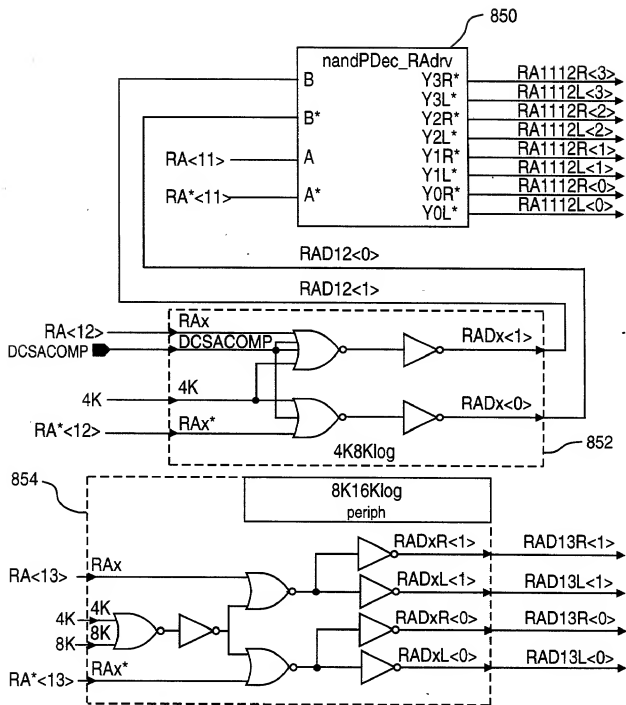


FIG. 50C

654

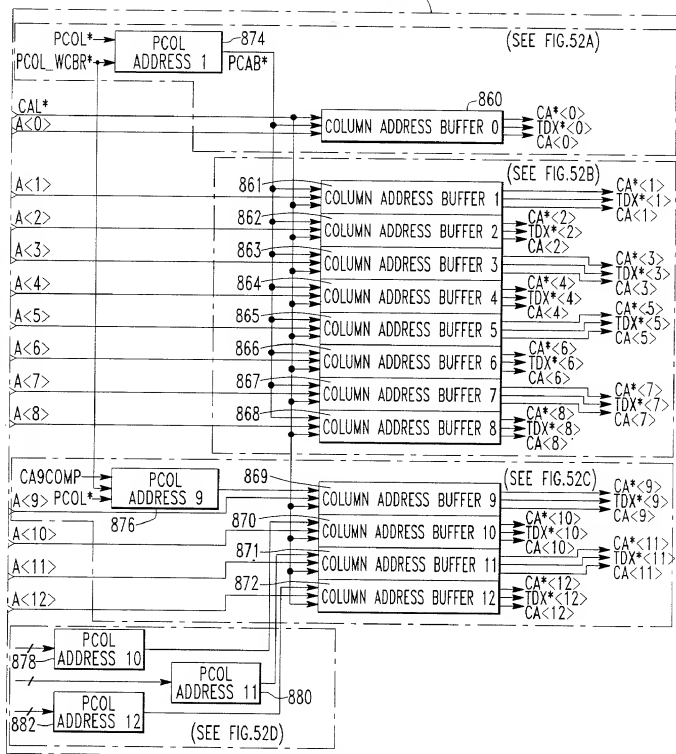


FIG. 51A

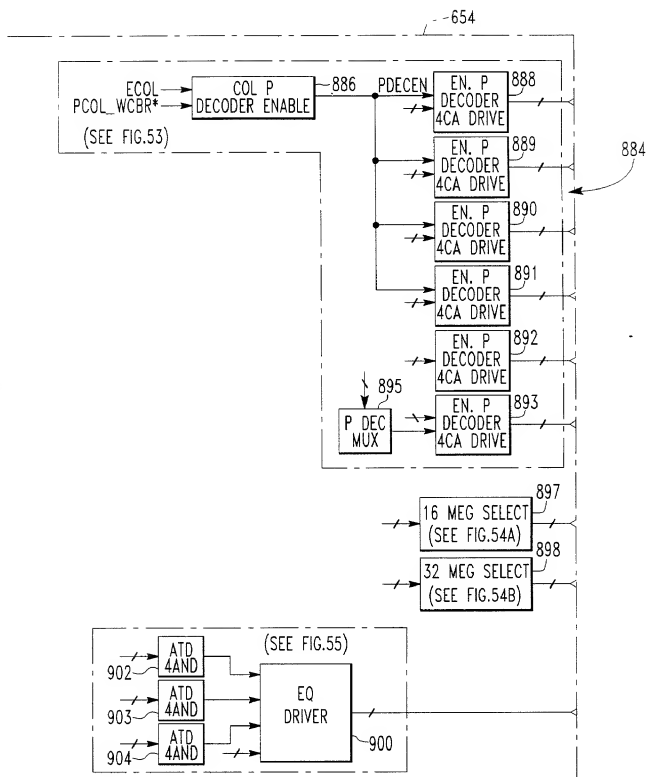


FIG. 51B

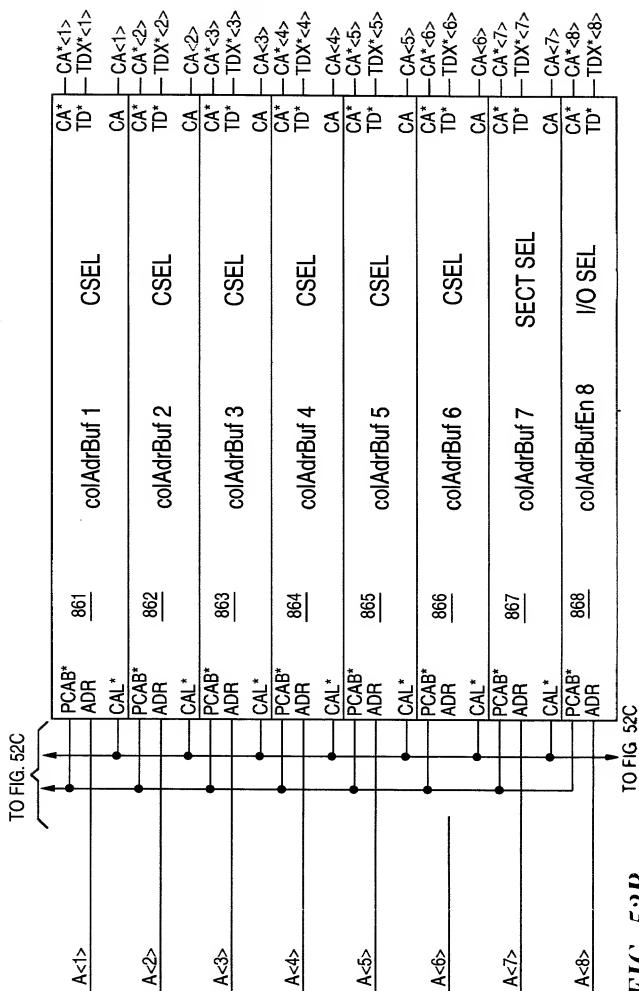


FIG. 52B

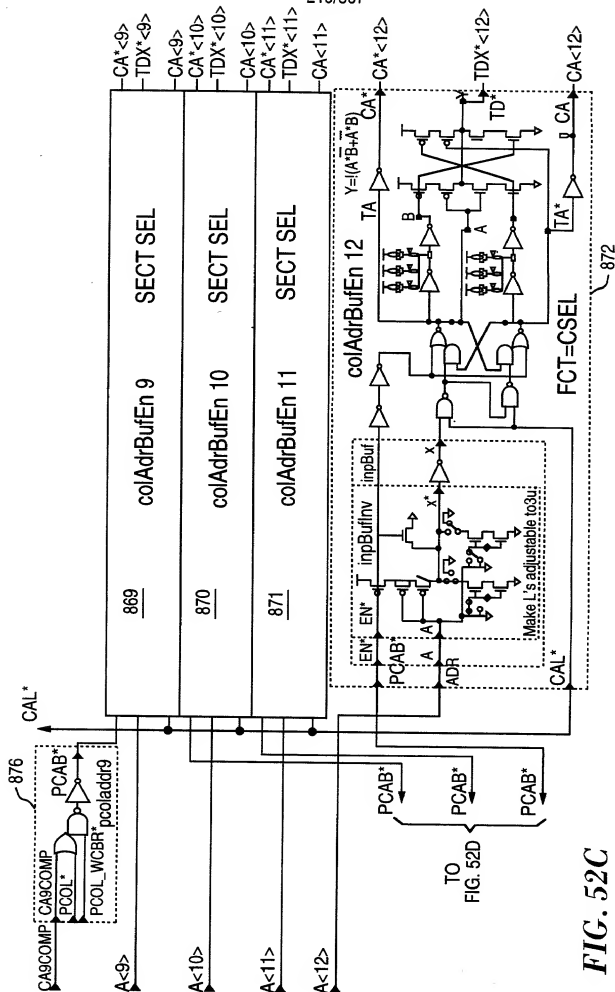


FIG. 52C

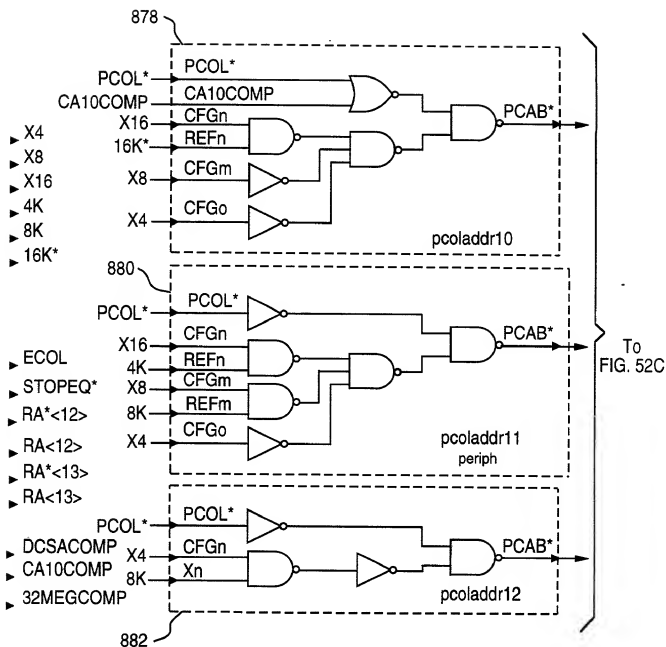


FIG. 52D

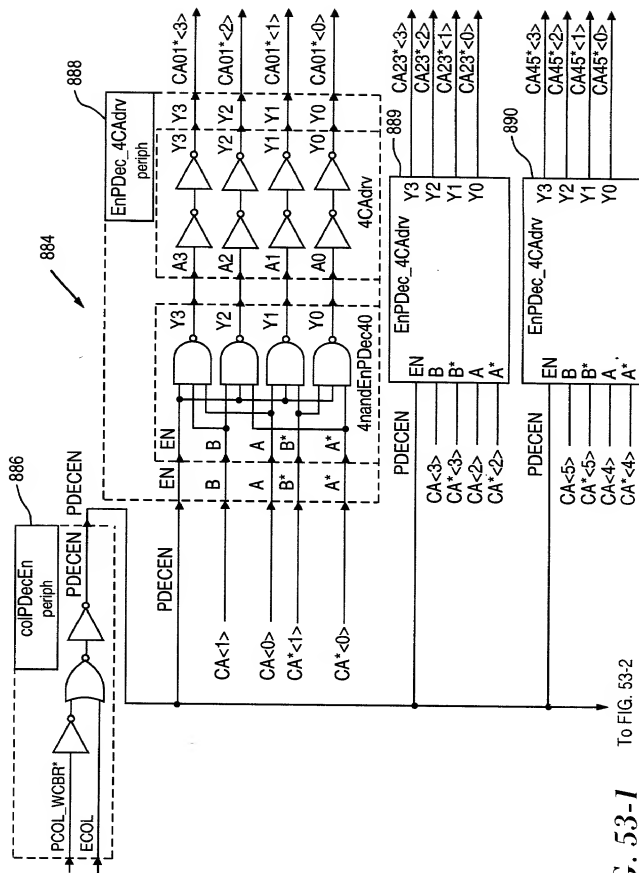


FIG. 53-1 To FIG. 53-2

To FIG. 53-1

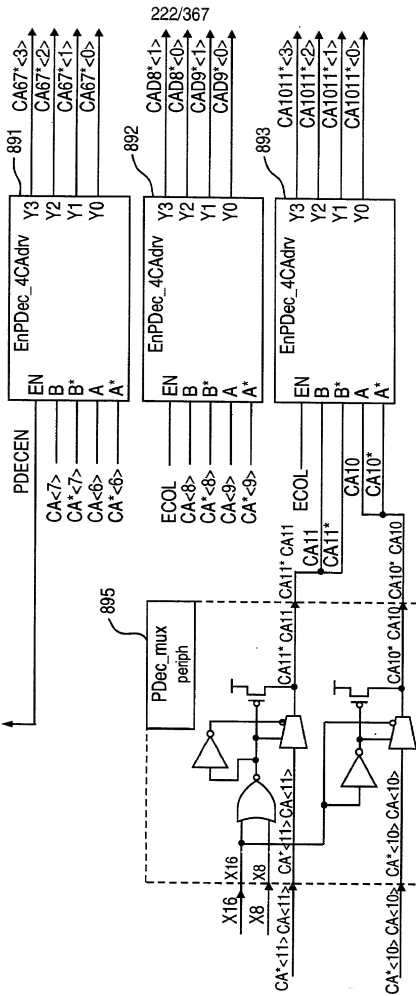
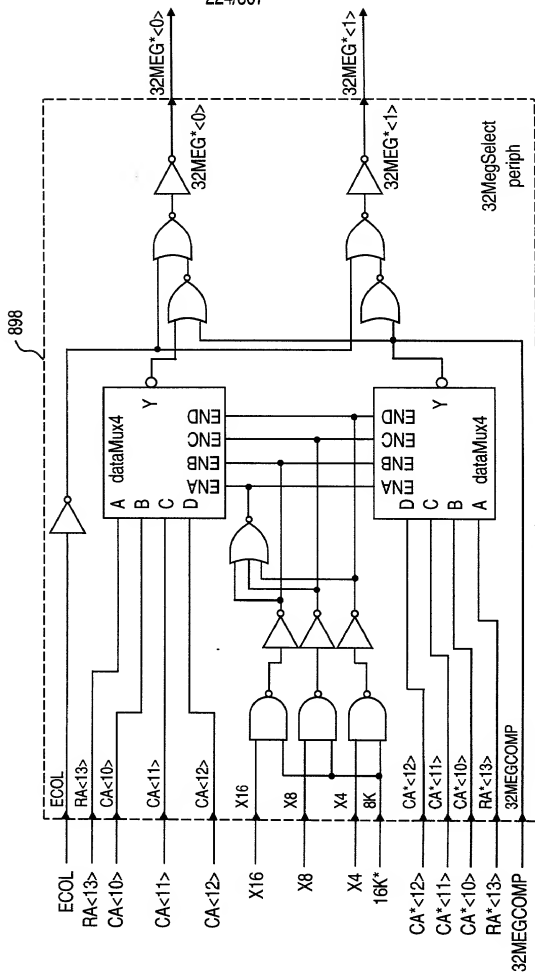


FIG. 53-2



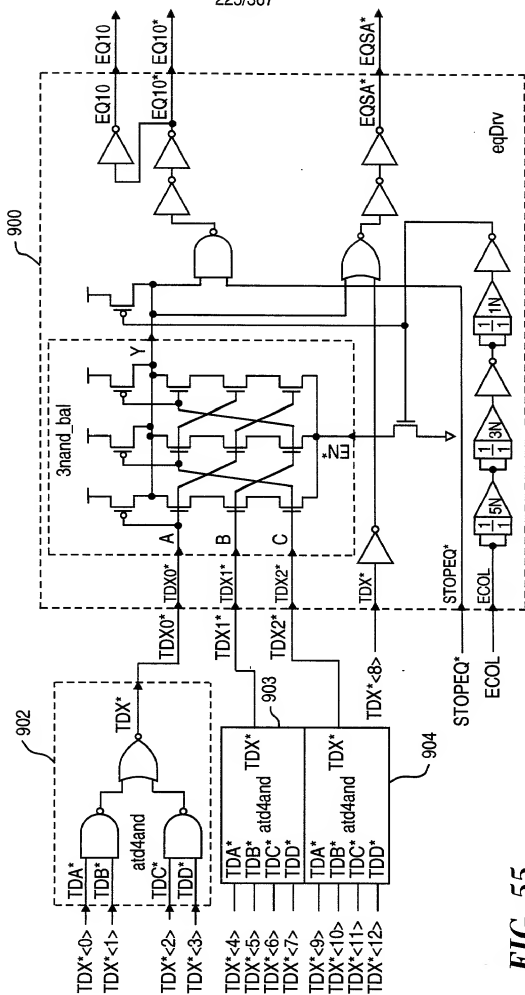


FIG. 55

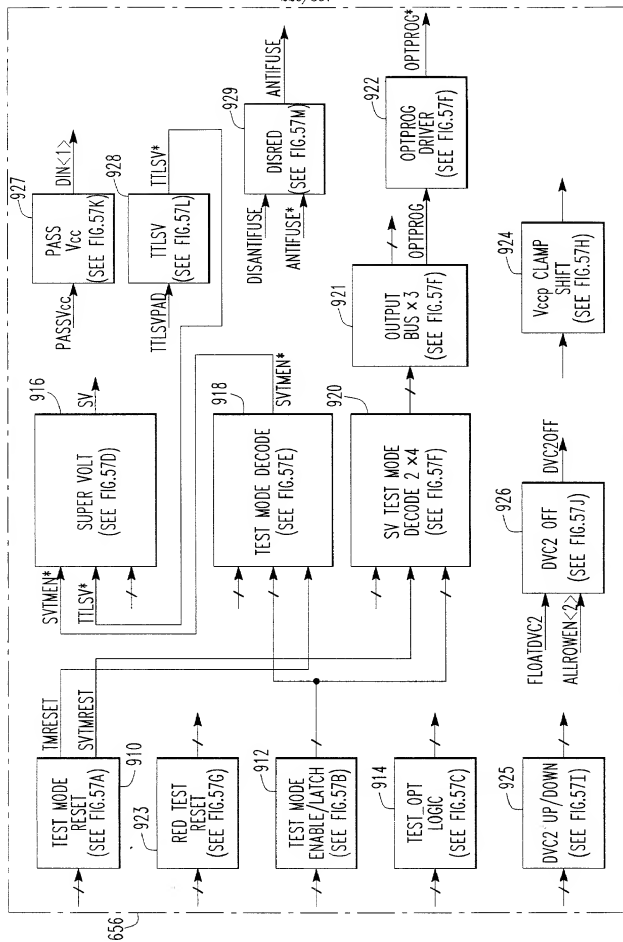


FIG. 56

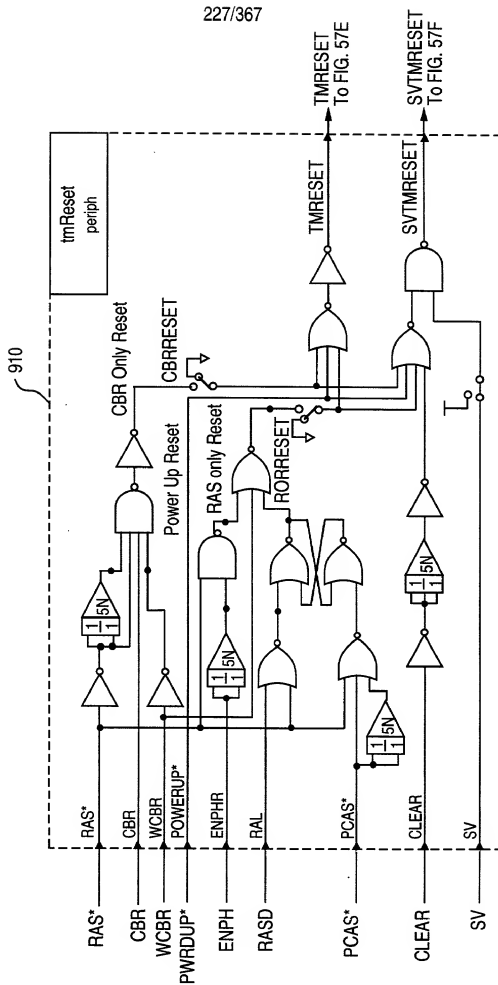


FIG. 57A

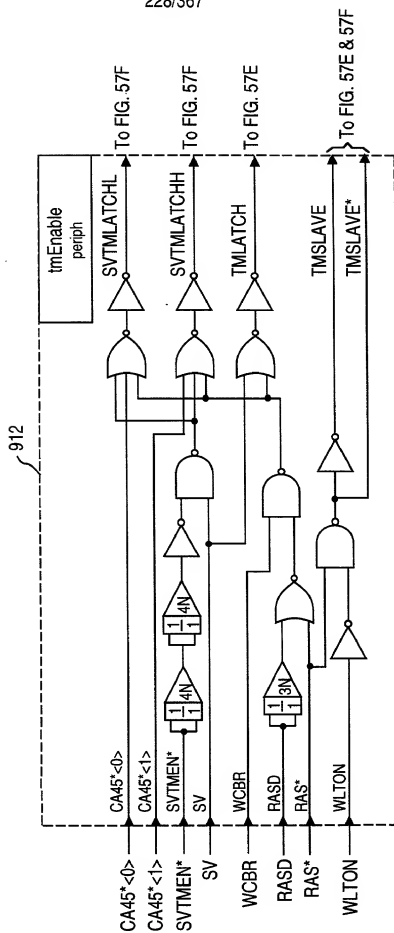


FIG. 57B

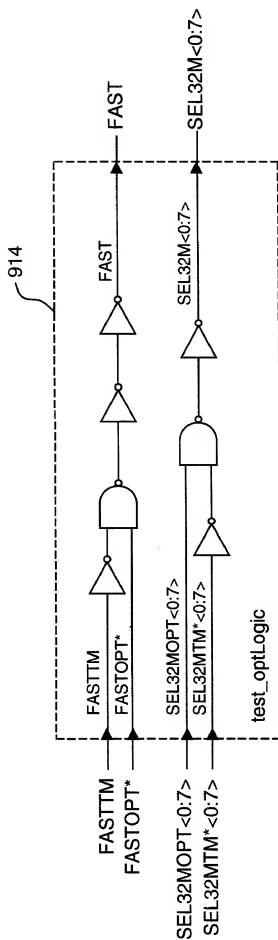
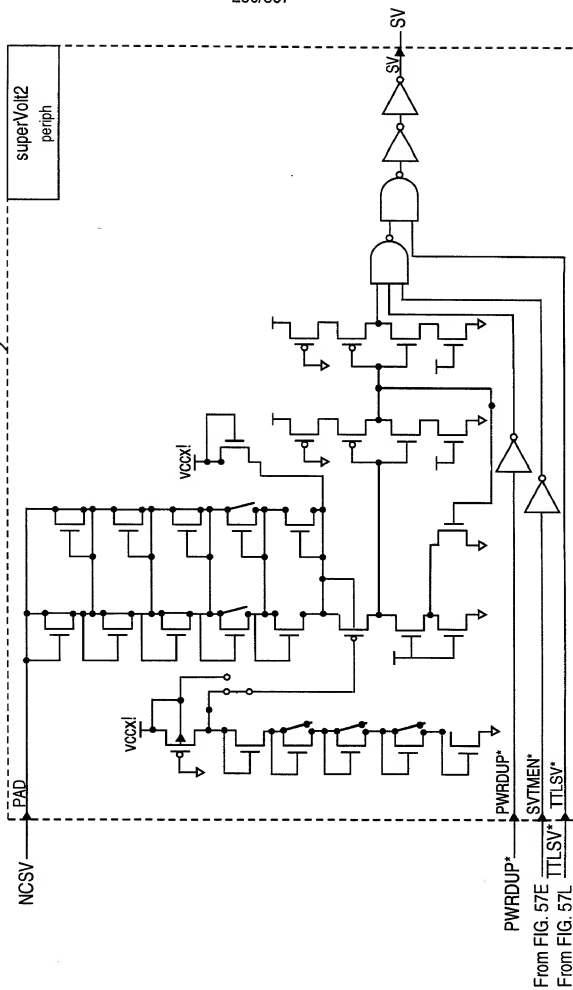


FIG. 57C

916



From FIG. 57E
From FIG. 57L

FIG. 57D

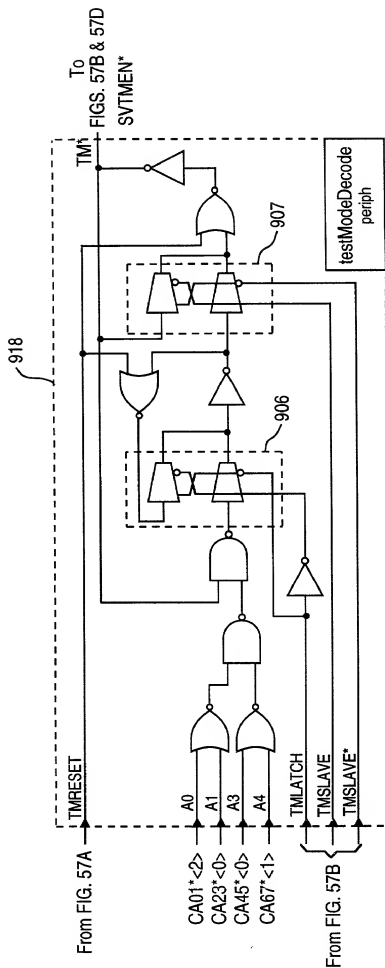


FIG. 57E



To
FIG. 57F-3

FIG. 57F-1



FIG. 57F-2

FIG. 57F-1

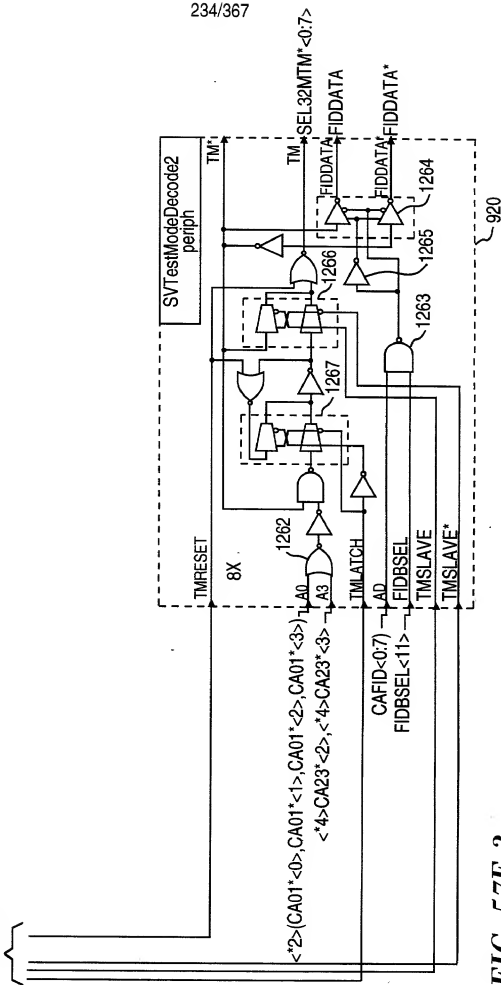
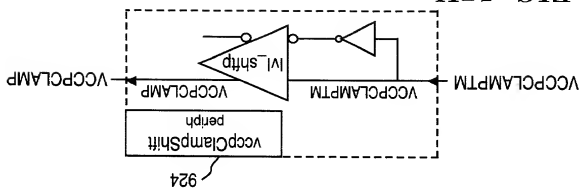
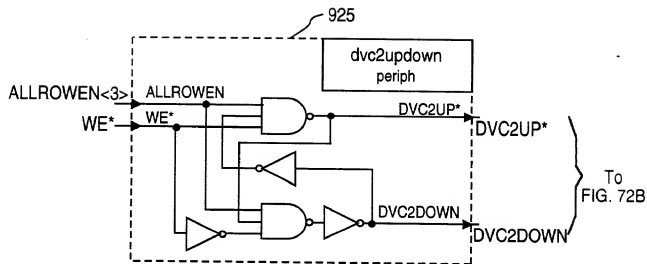
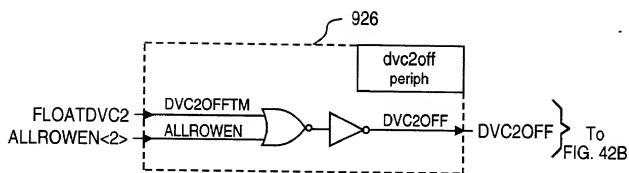


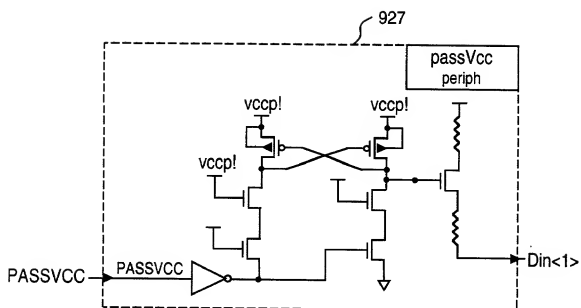
FIG. 57F-3

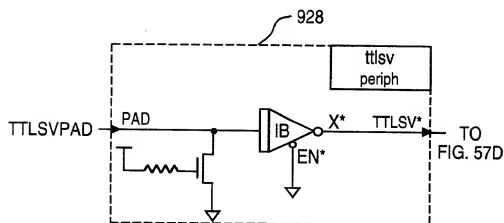
FIG. 57H

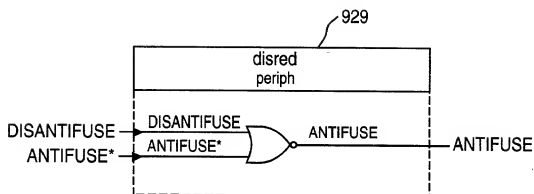


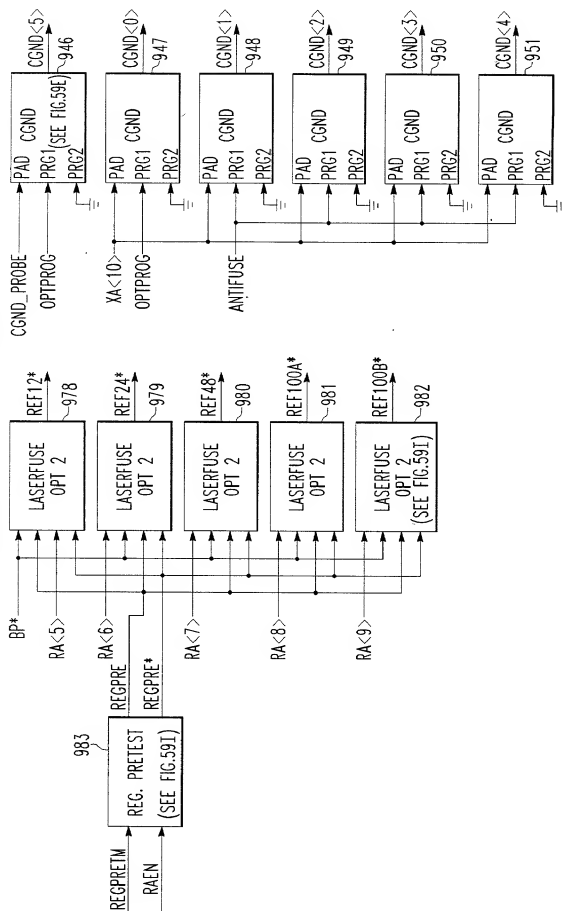
**FIG. 57I**

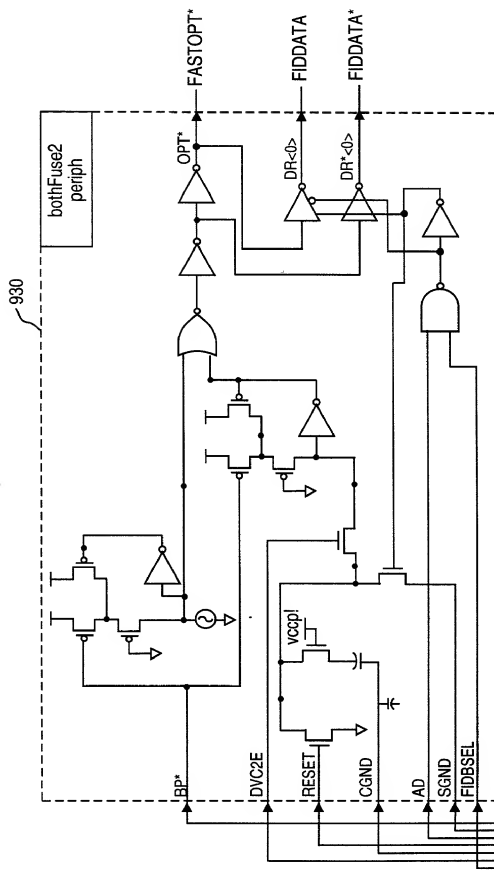
**FIG. 57J**

**FIG. 57K**

**FIG. 57L**

**FIG. 57M**





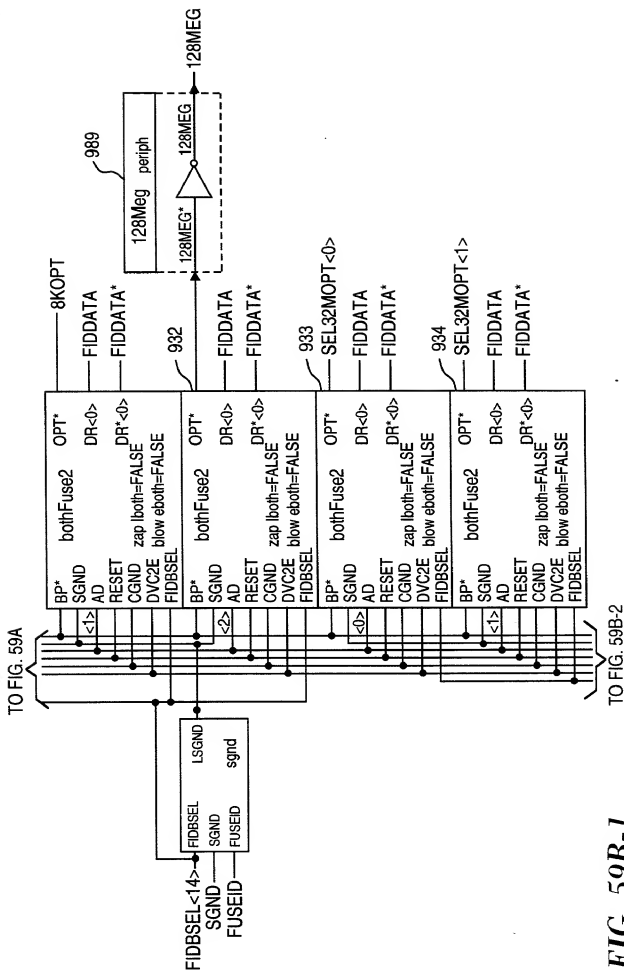


FIG. 59B-1

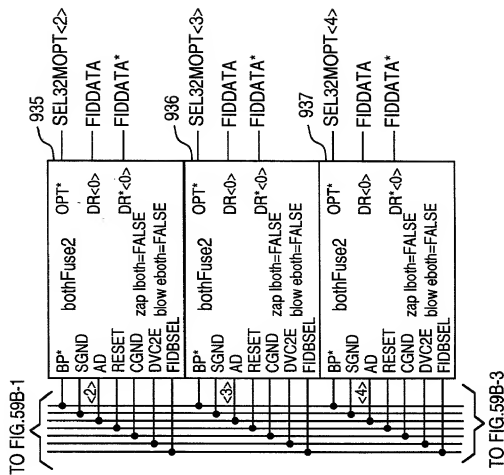


FIG. 59B-2

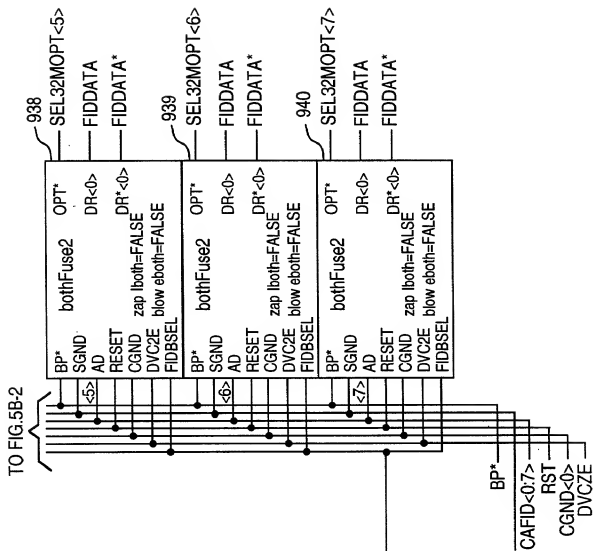
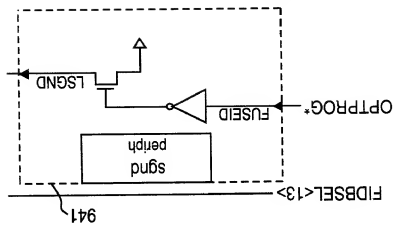


FIG. 59B-3

FIG. 59C



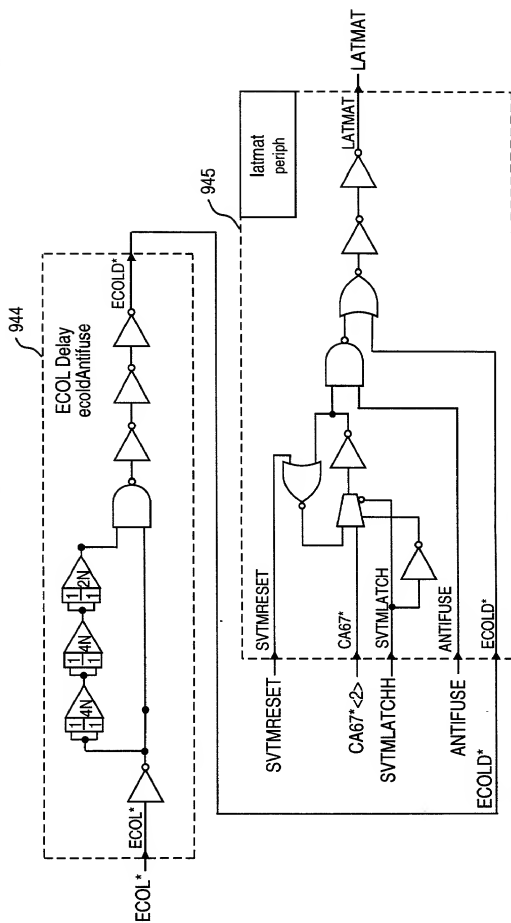


FIG. 59D

00001620 000001
100000 00010000

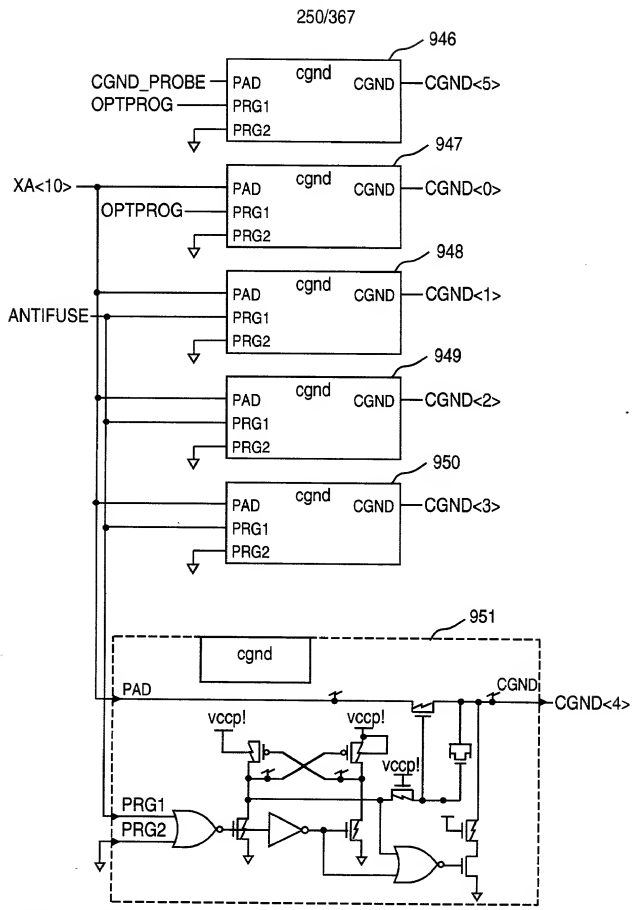
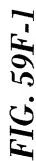
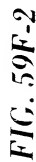


FIG. 59E





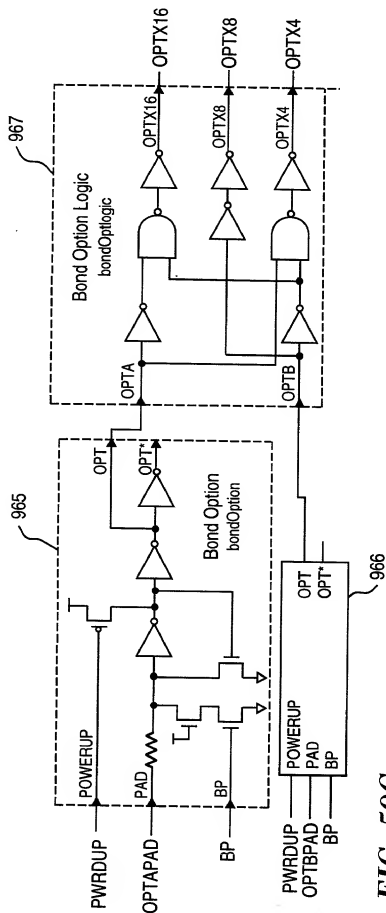
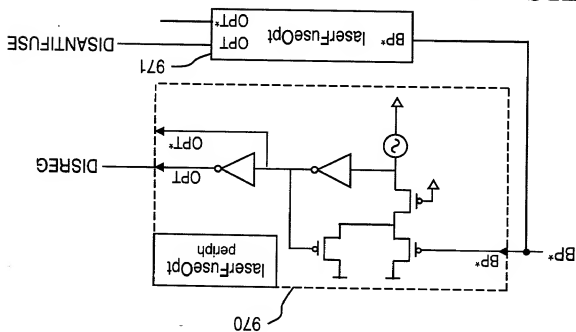
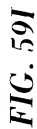
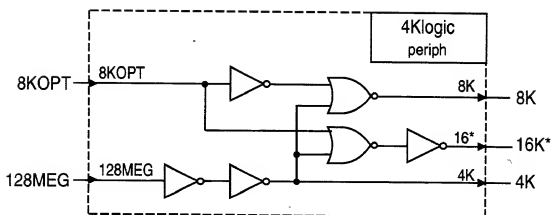


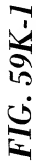
FIG. 59C

FIG. 59H





**FIG. 59J**



108050" 82510860

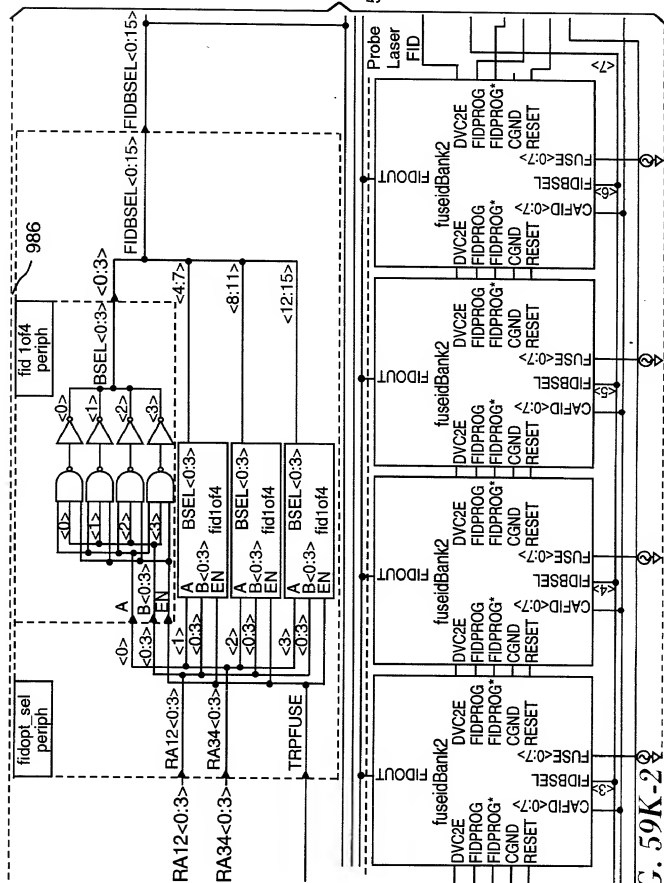


FIG. 59K-2

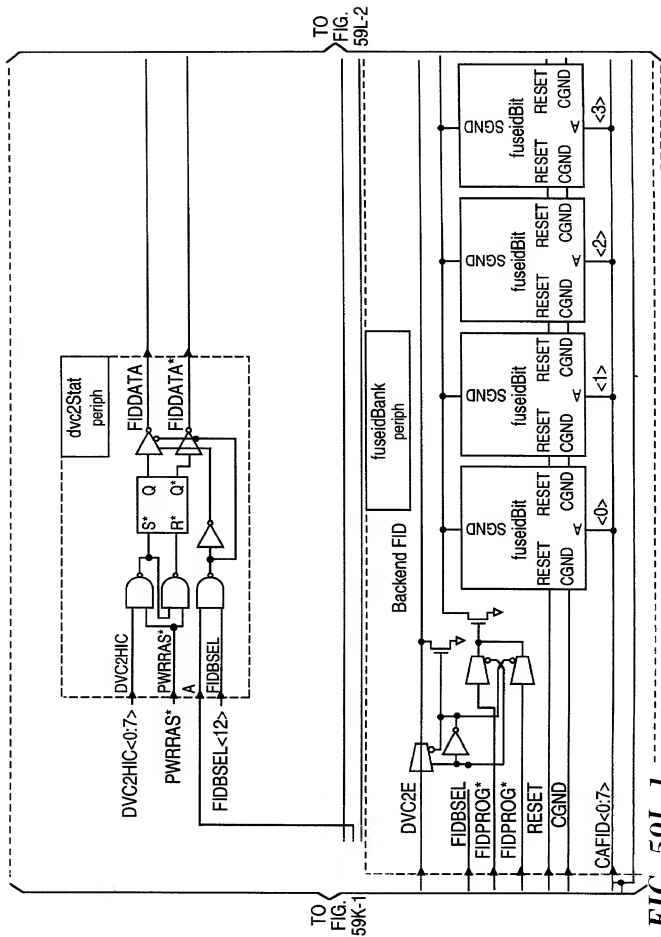
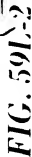
TO
FIG.
59L-2TO
FIG.
59K-1

FIG. 59L-1



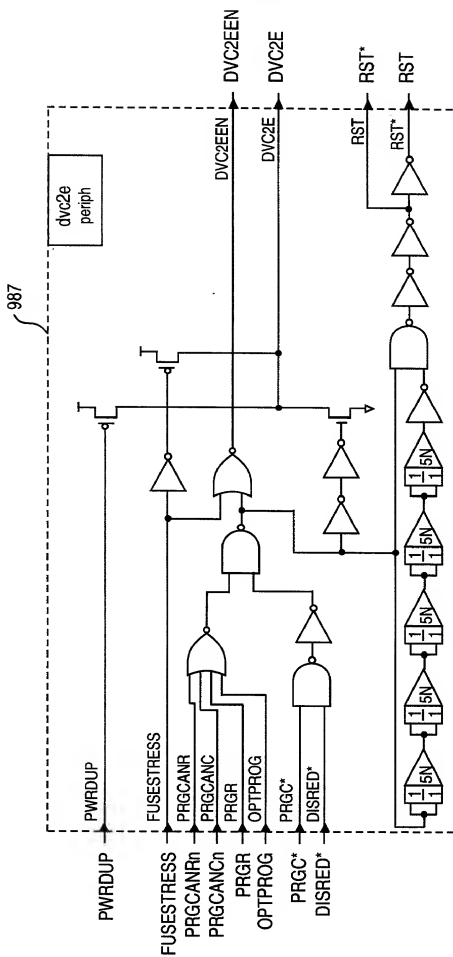
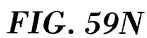


FIG. 59M



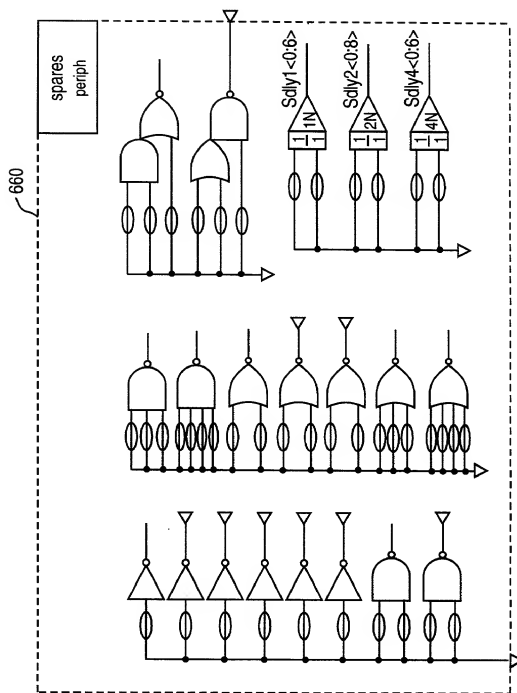


FIG. 590

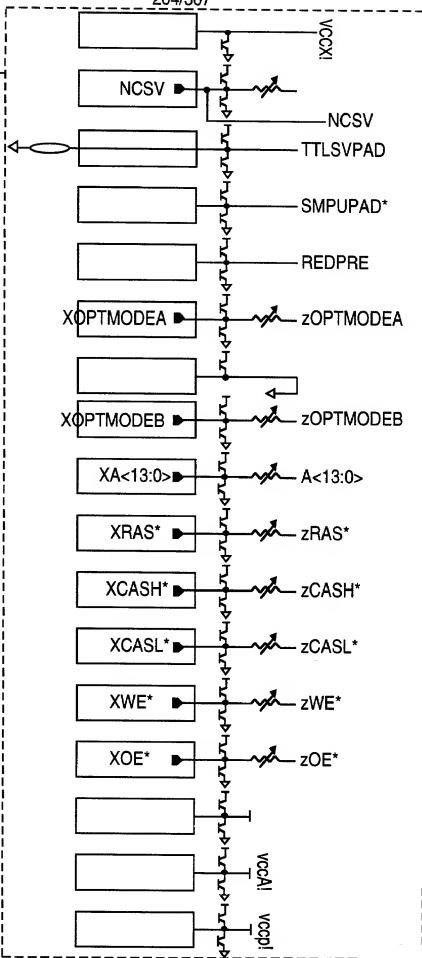


FIG. 59P

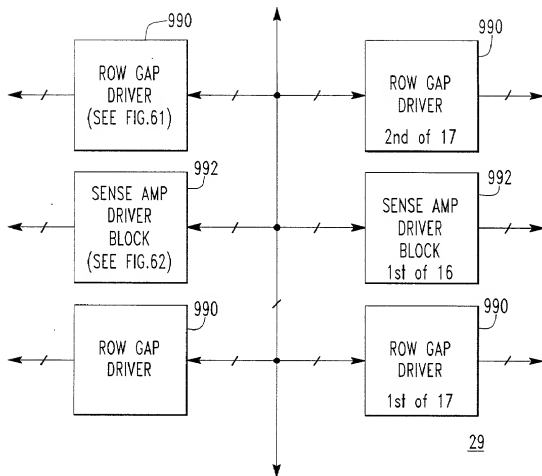


FIG. 60

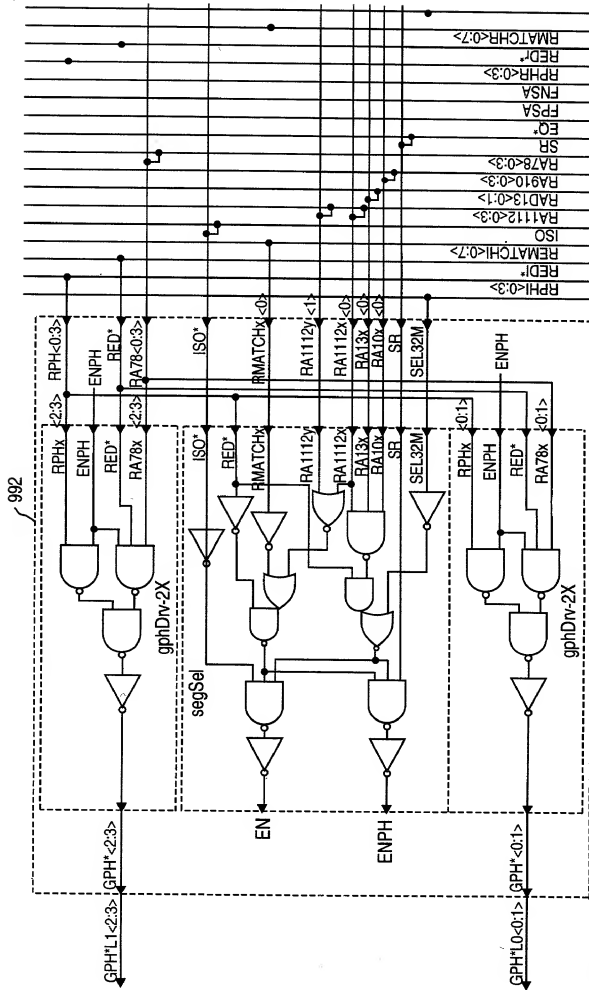


FIG. 61



FIG. 62

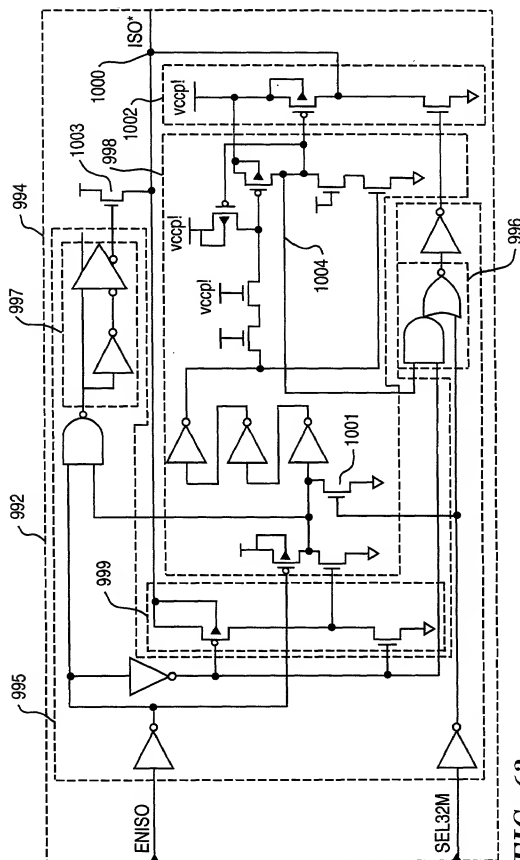


FIG. 63

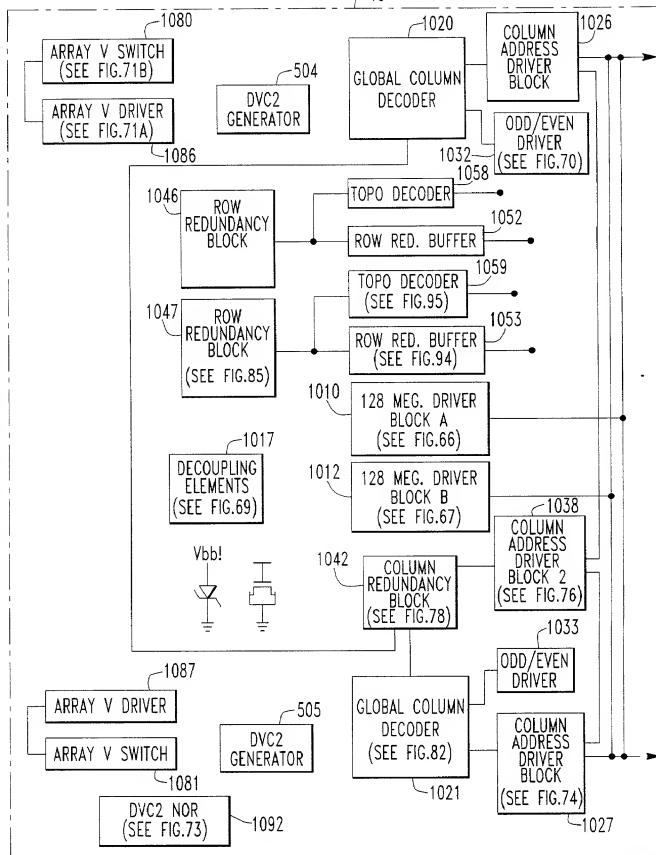


FIG. 64A

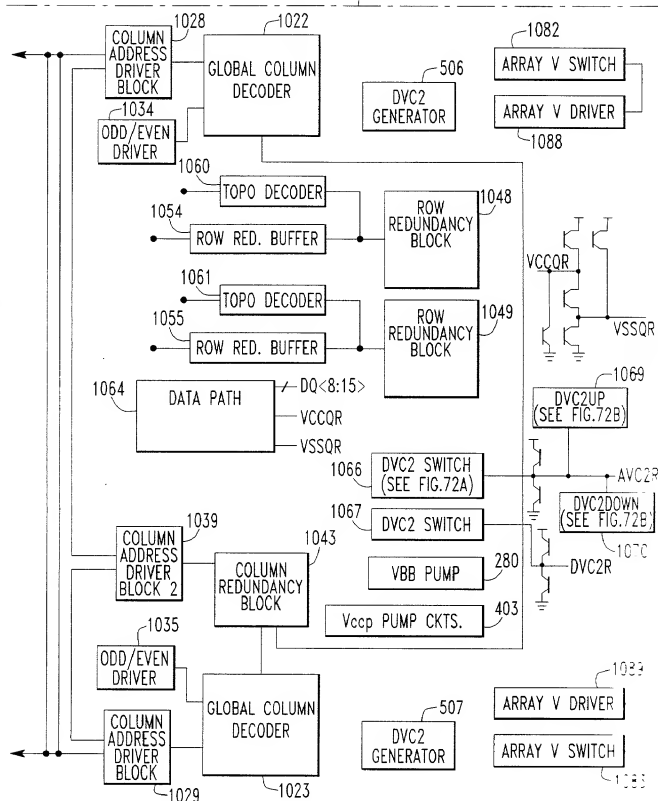


FIG. 64B

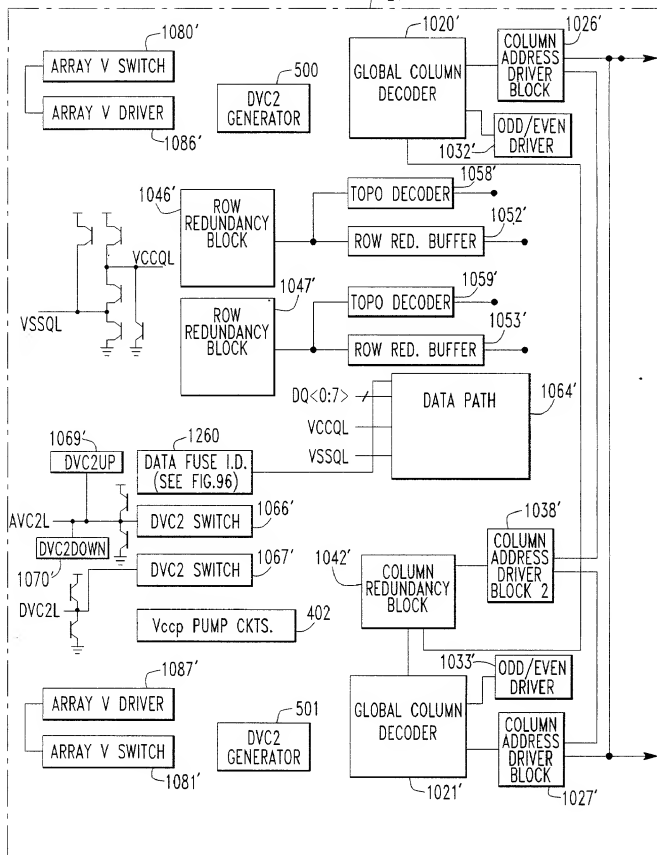


FIG. 65A

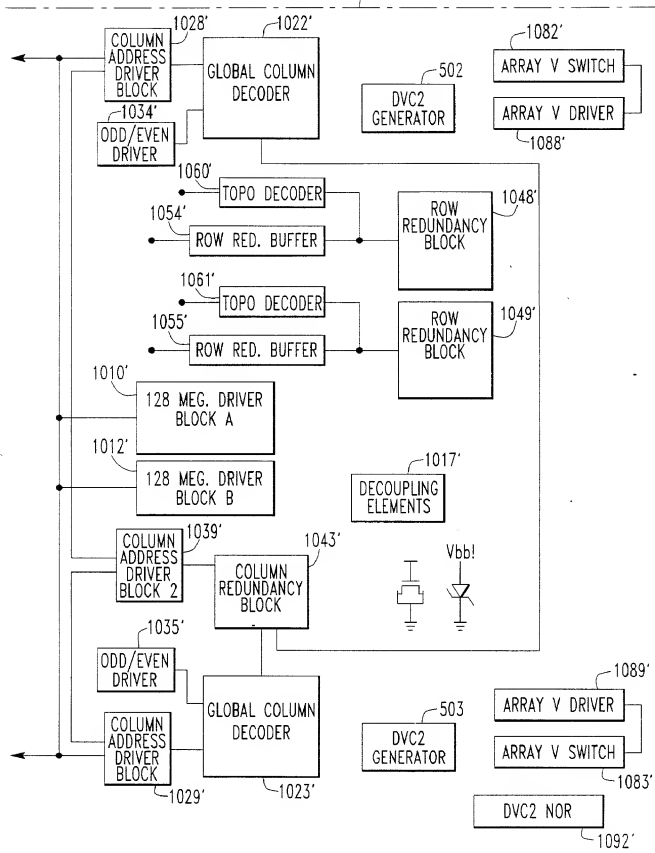


FIG. 65B

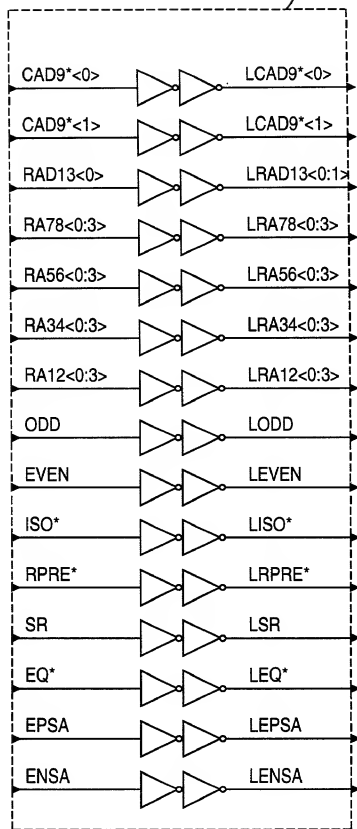


FIG. 66

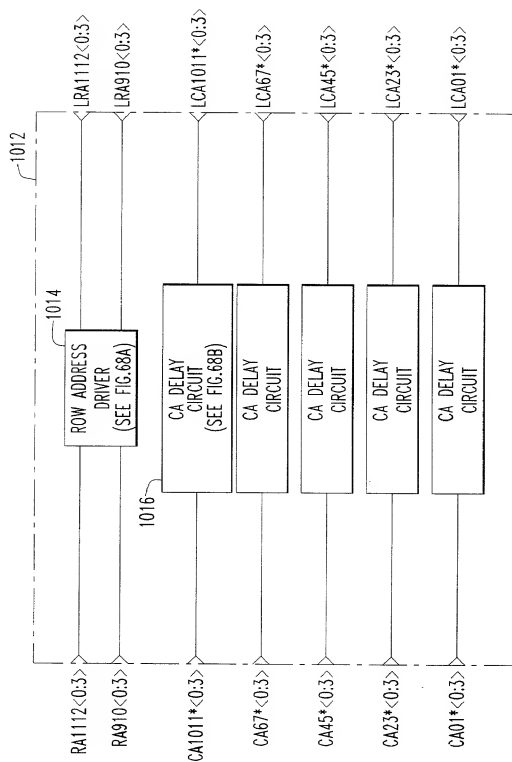
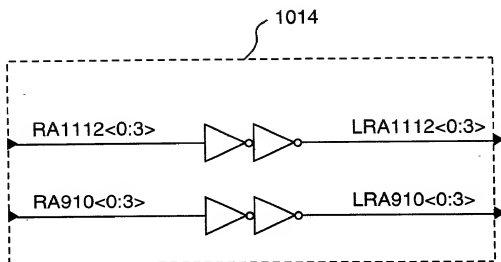
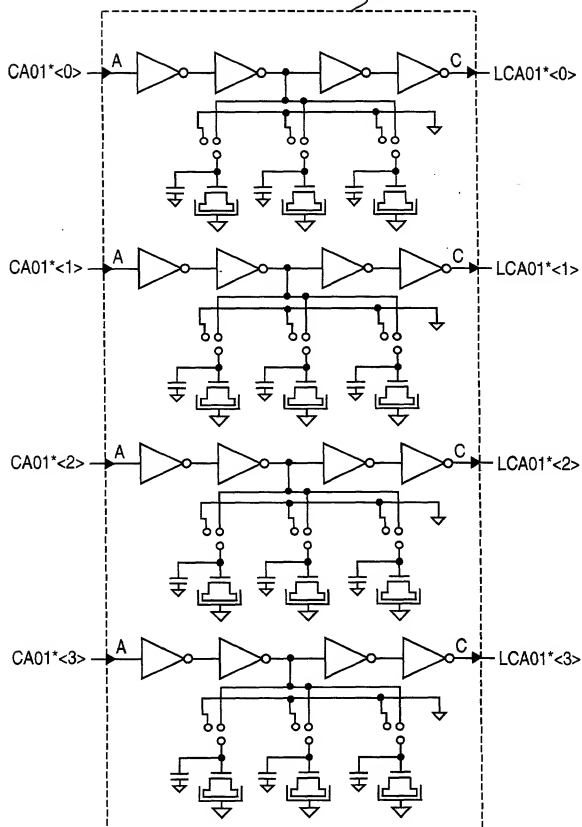
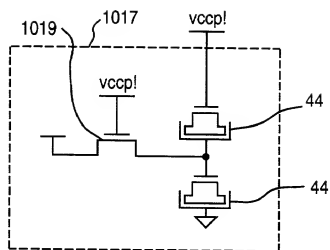
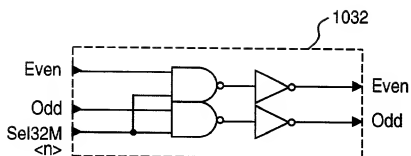


FIG. 67

**FIG. 68A**

**FIG. 68B**

**FIG. 69**

**FIG. 70**

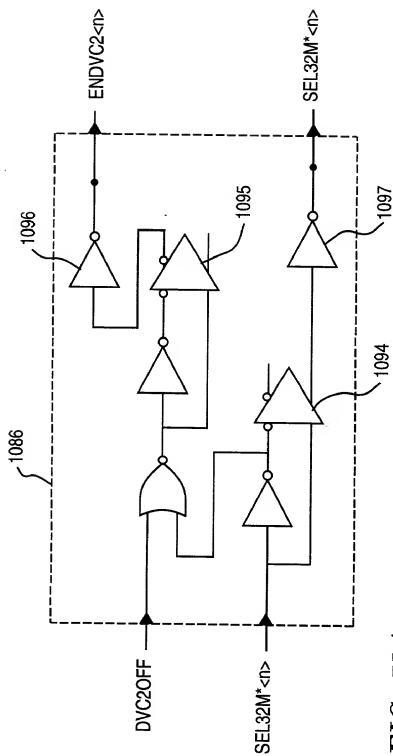


FIG. 71A

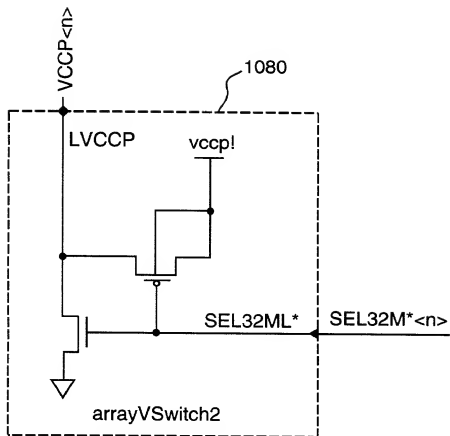
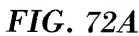
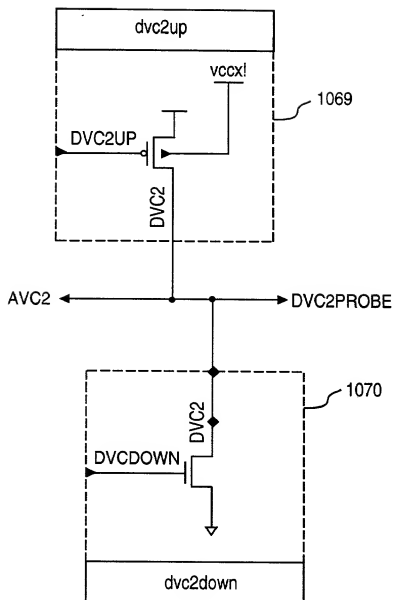
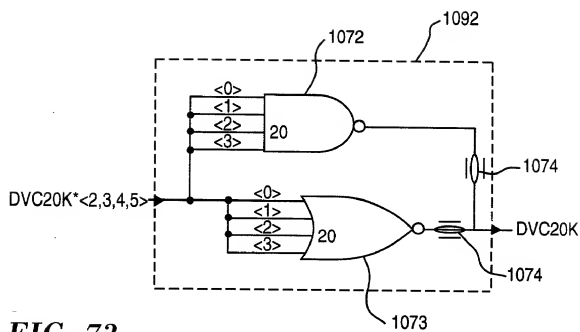


FIG. 71B



**FIG. 72B**

**FIG. 73**

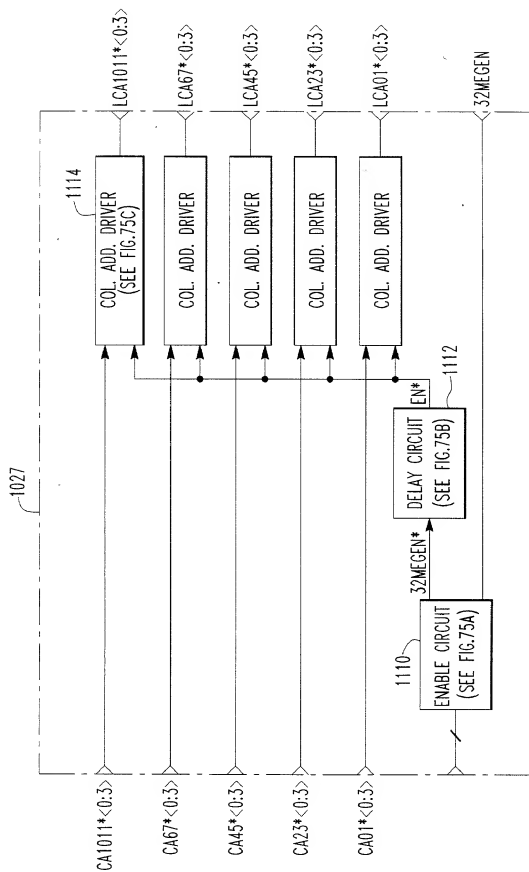


FIG. 74

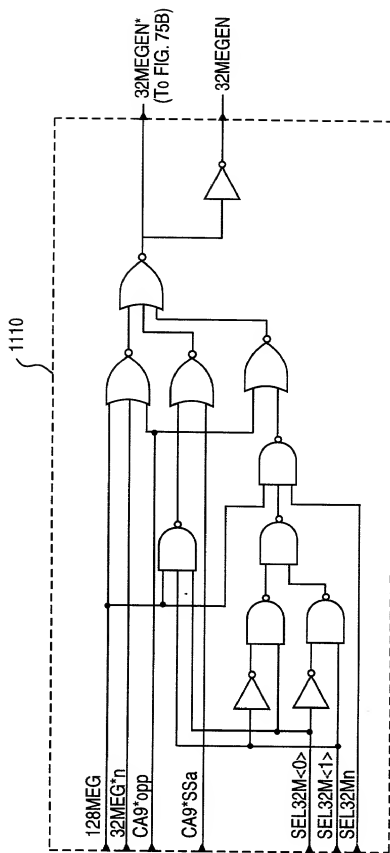


FIG. 75A

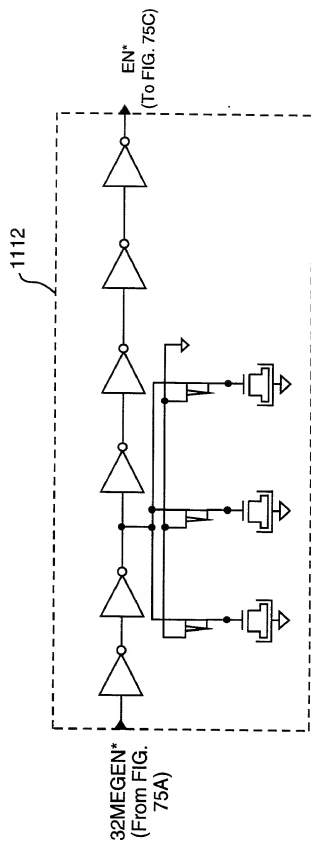


FIG. 75B

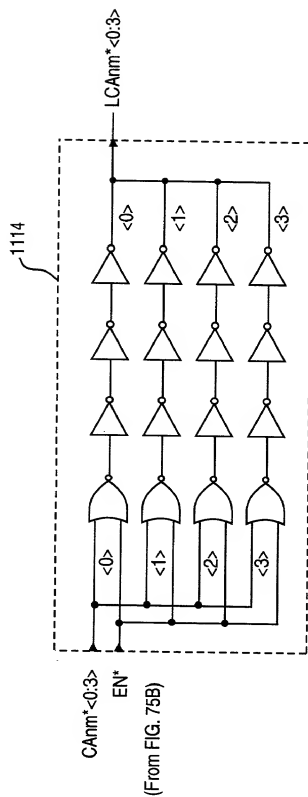


FIG. 75C

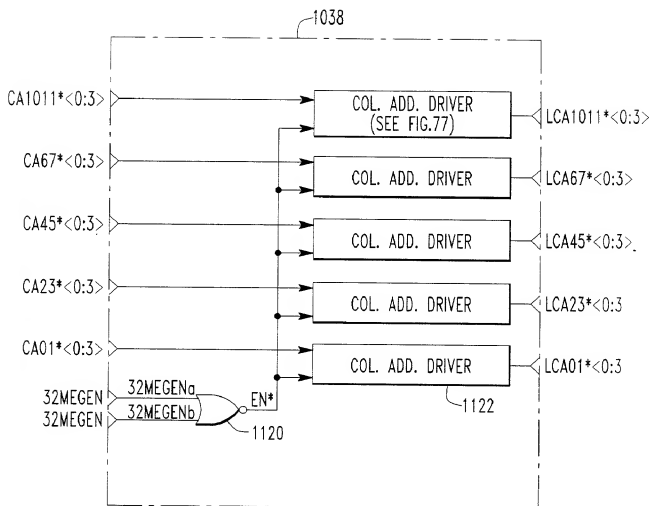


FIG. 76

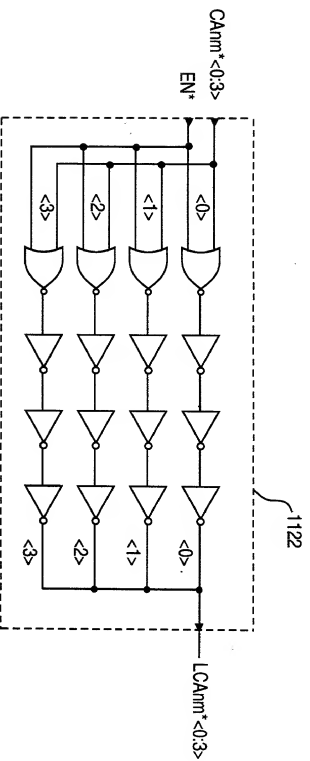


FIG. 77

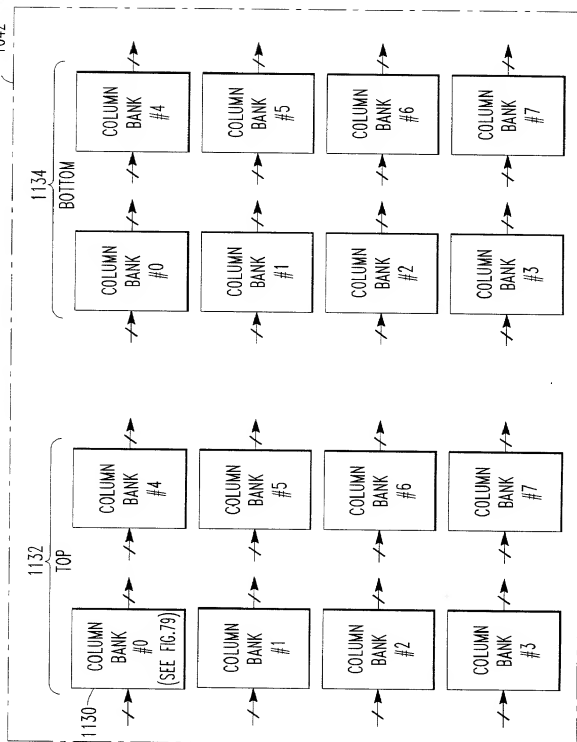


FIG. 78

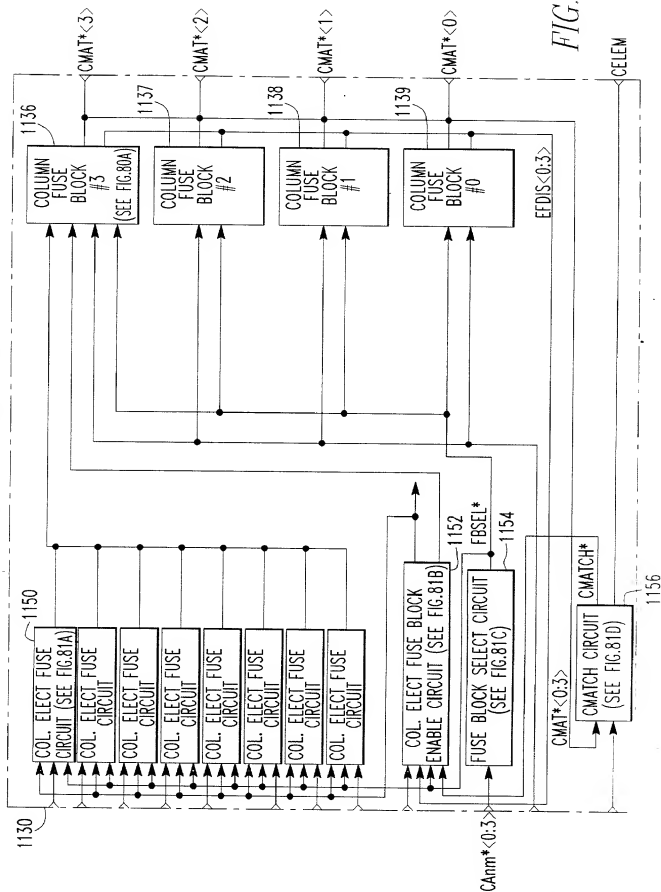


FIG. 79

FIG. 80C is a block diagram of a programmable logic device. It consists of four parallel processing blocks (1144) and an enable circuit (1146). Each block 1144 takes inputs from PR0, PR1, and CA01* (or PR2, PR3, CA23*, etc.) and outputs CAM* and CFP/CFP*. The enable circuit 1146 takes inputs from PR0, PR1, and CA01* (or PR2, PR3, CA23*, etc.) and outputs EN. The CAM* signals are connected to an output circuit (1148) which also receives CAMAT*n and outputs (SEE FIG. 80B).

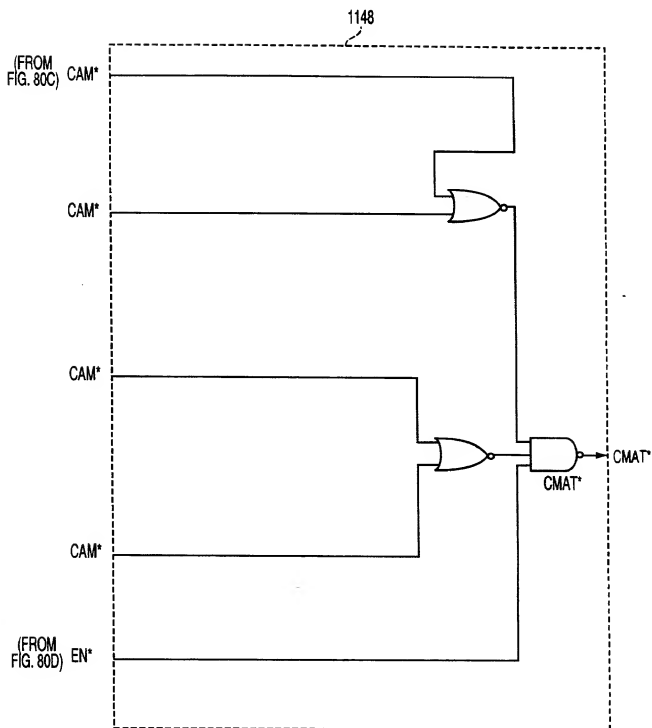


FIG. 80B

CAM*
(TO FIG. 80B)

1144

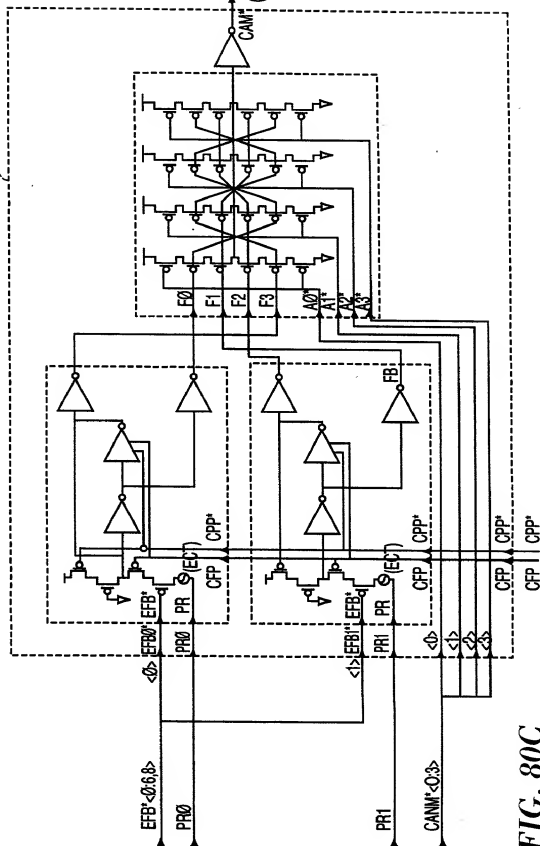


FIG. 80C

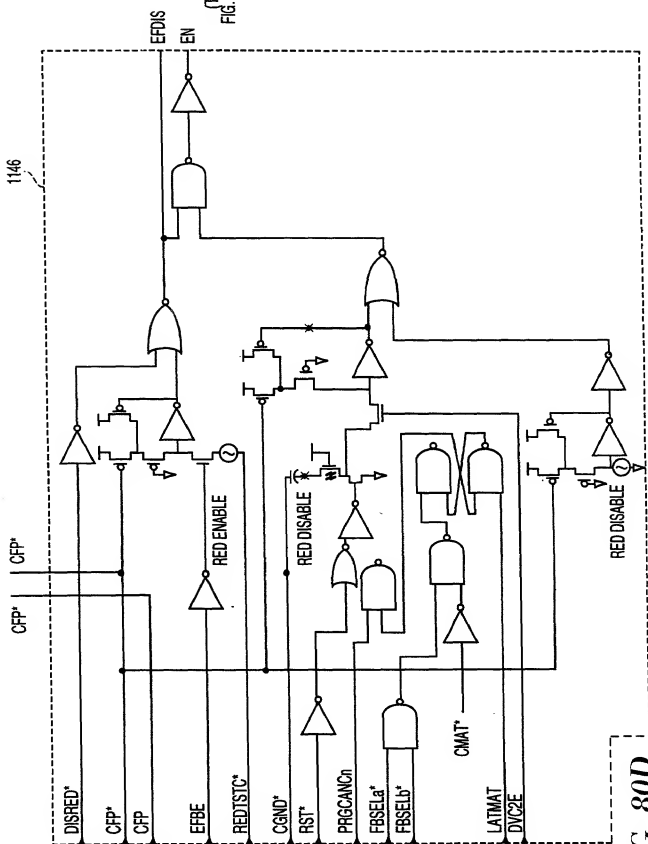


FIG. 80D

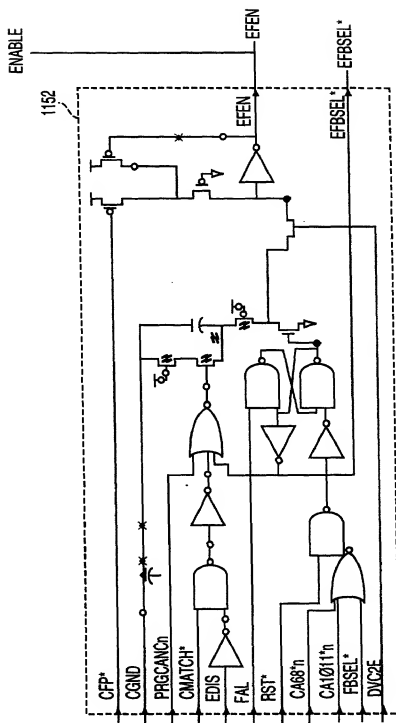


FIG. 81B

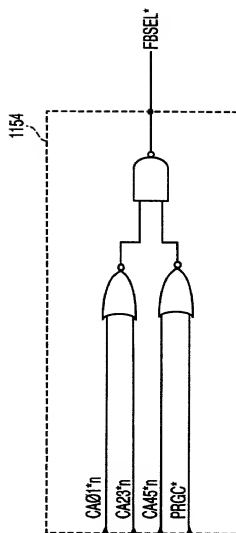


FIG. 81C

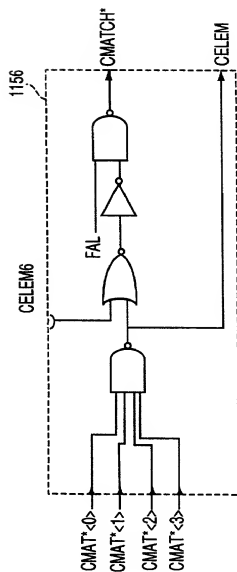


FIG. 81D

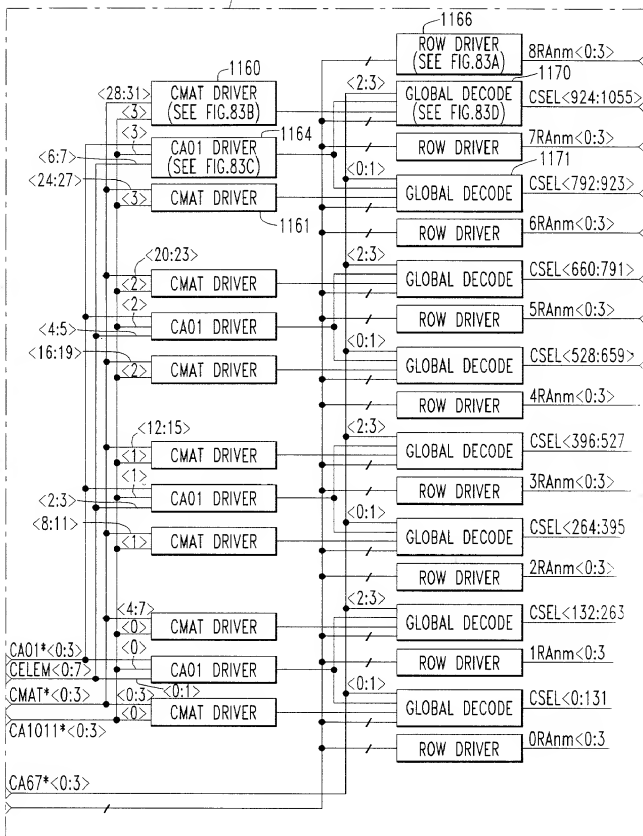


FIG. 82

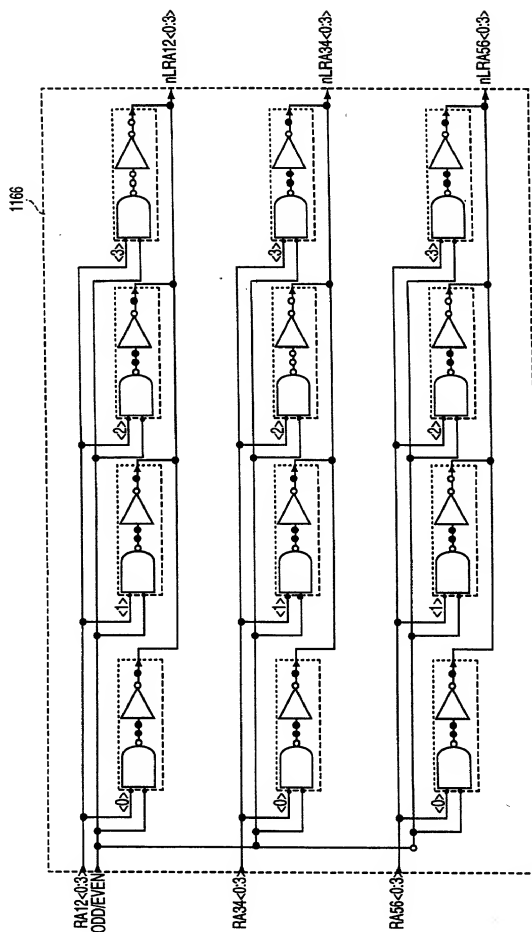


FIG. 83A

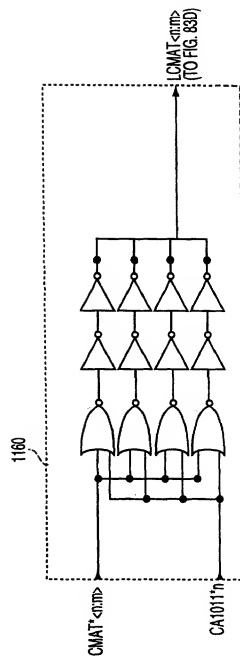


FIG. 83B

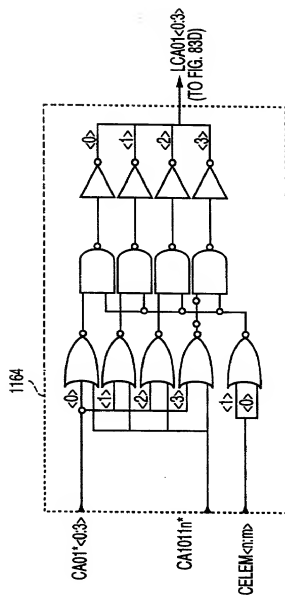
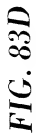


FIG. 83C



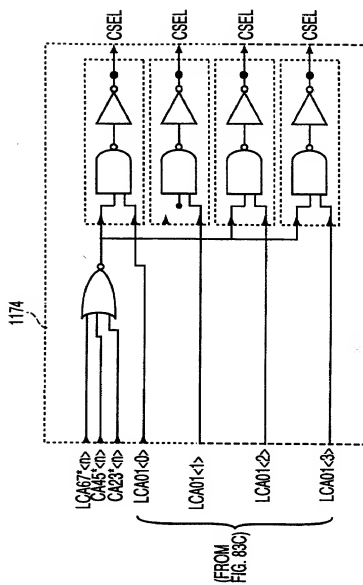
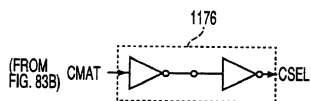


FIG. 84A

**FIG. 84B**

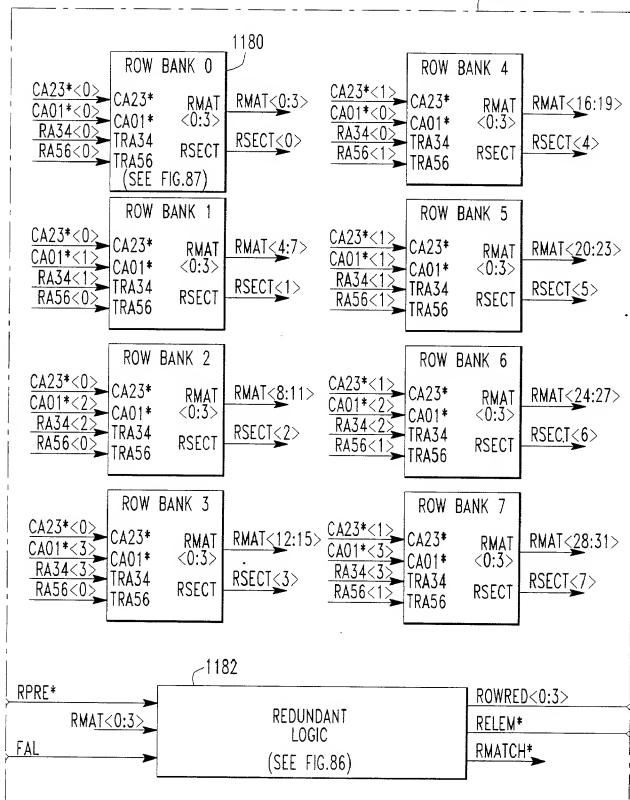


FIG. 85

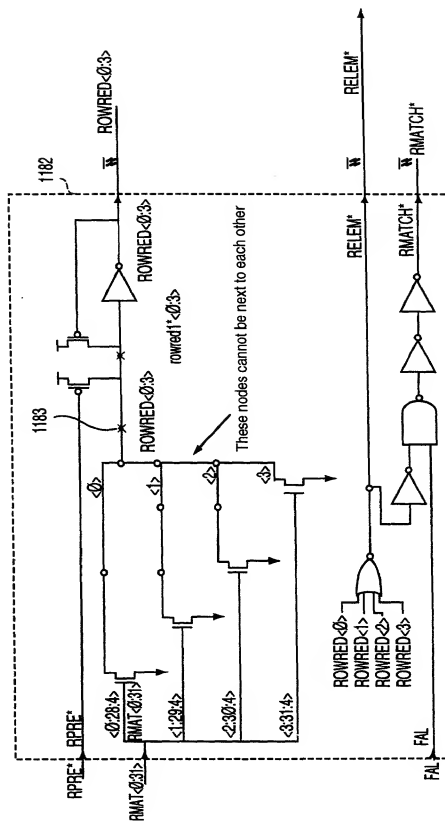


FIG. 86

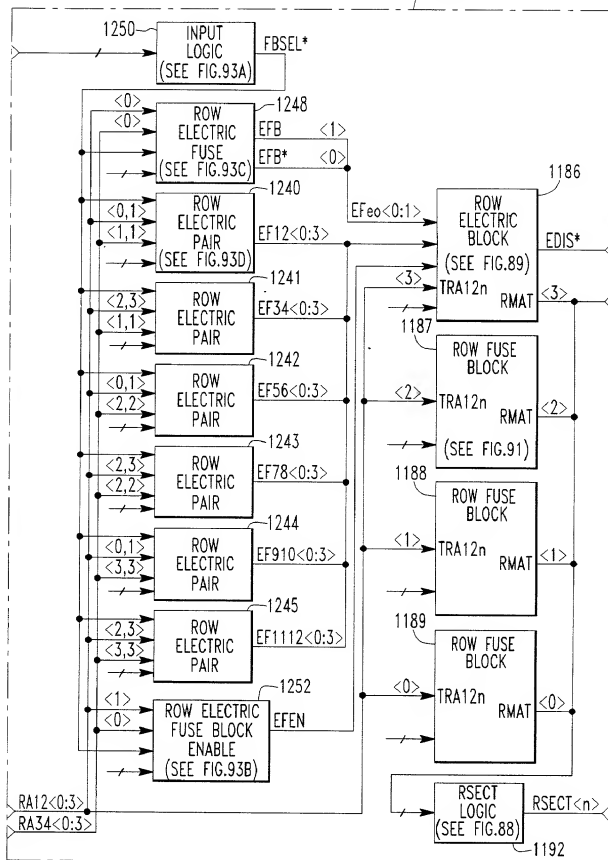
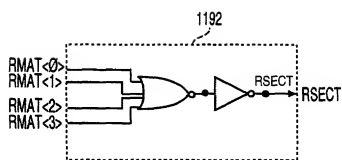


FIG. 87

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100	

**FIG. 88**

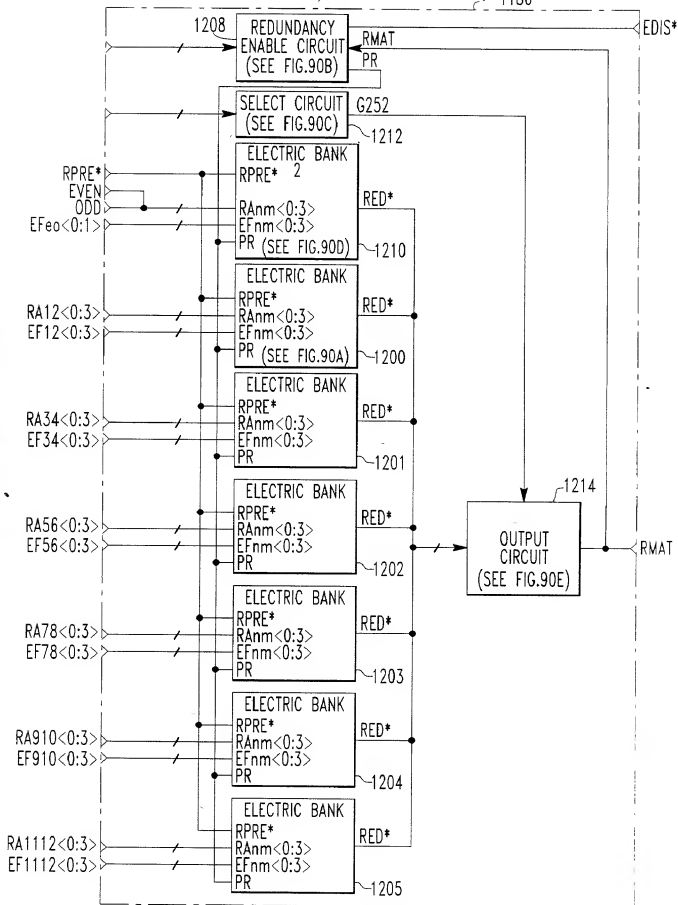


FIG. 89

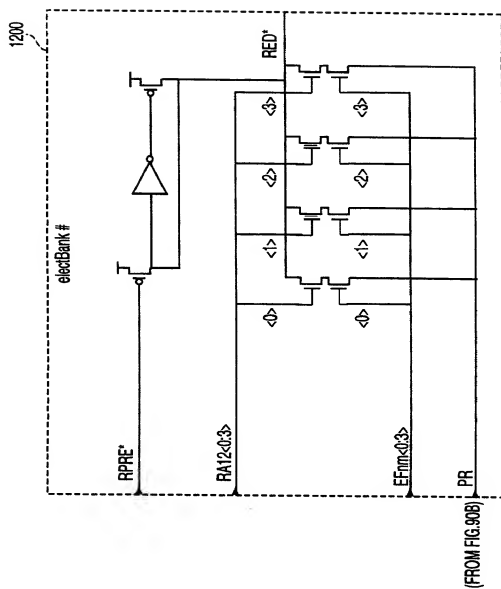


FIG. 90A

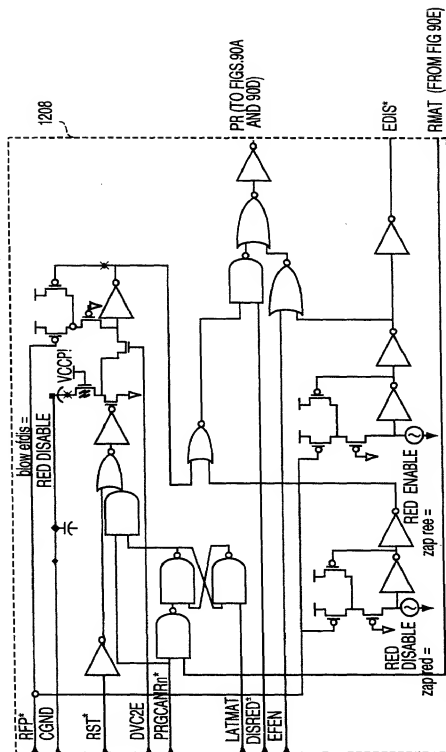


FIG. 90B

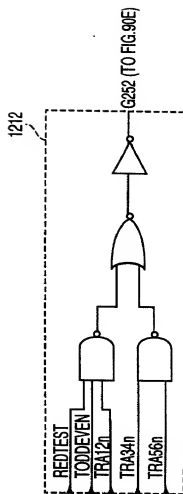


FIG. 90C

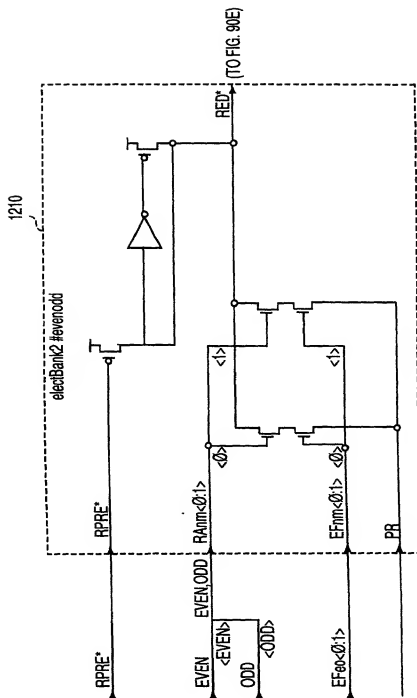


FIG. 90D

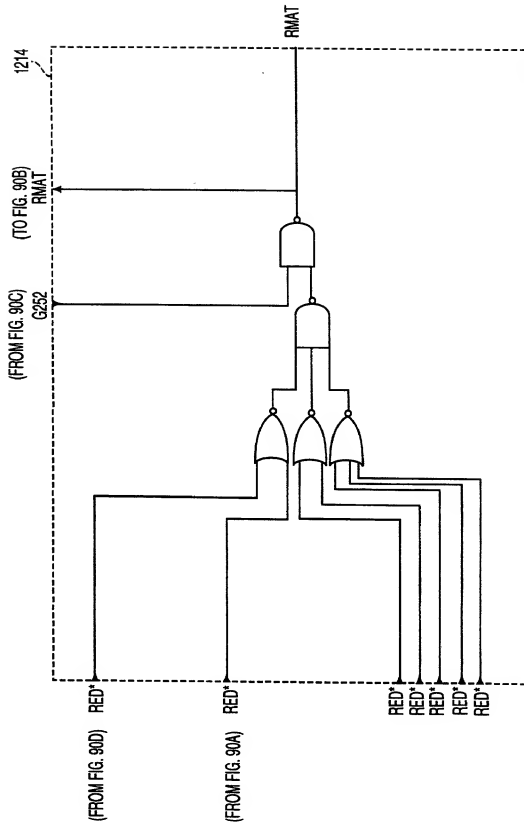
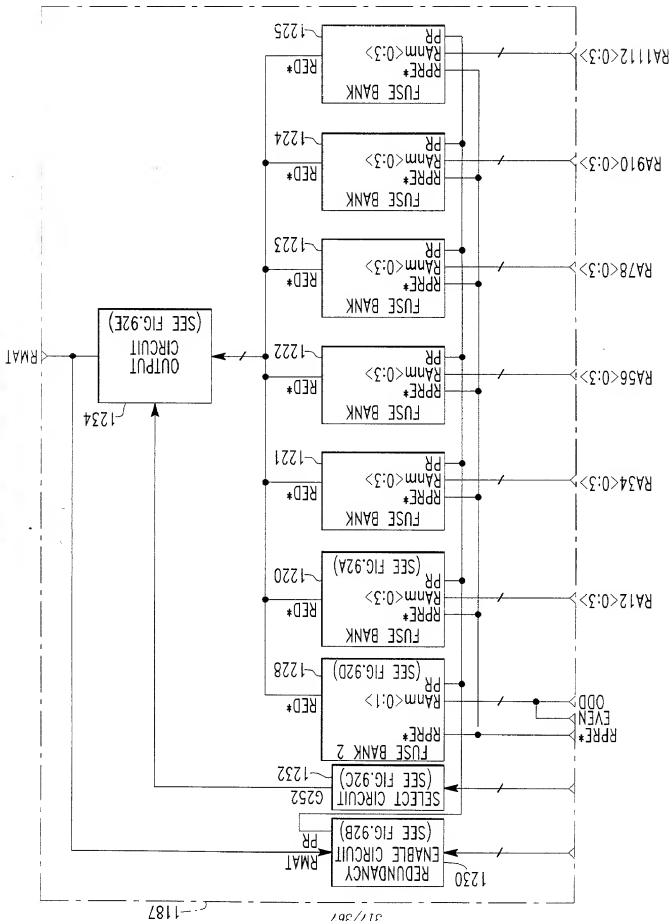


FIG. 90E

FIG. 91



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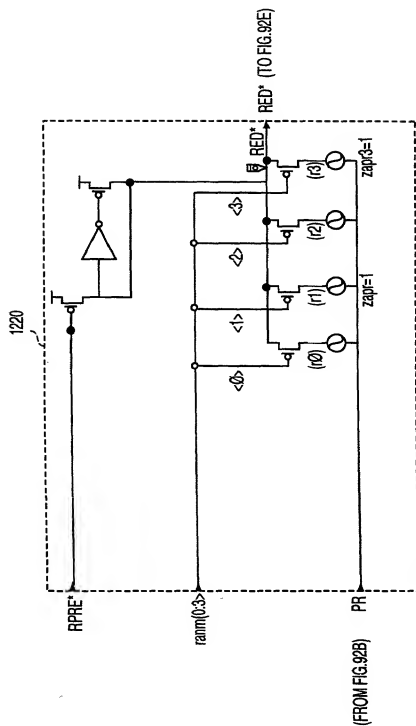


FIG. 92A

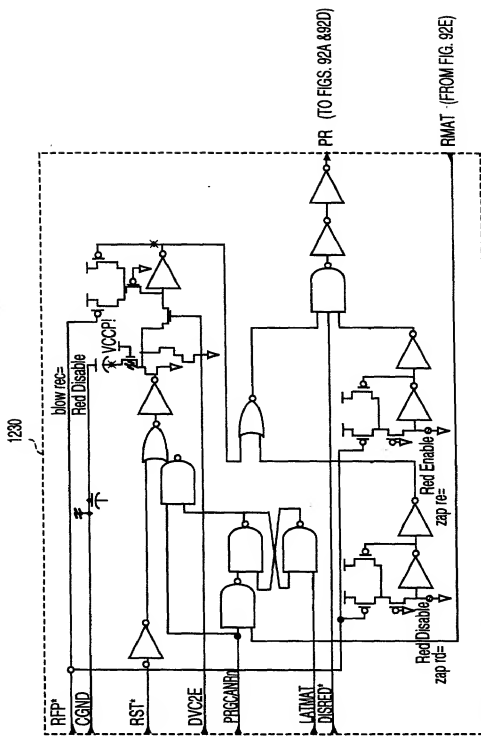
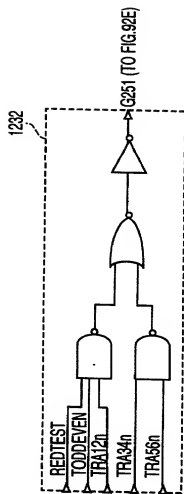


FIG. 92B

**FIG. 92C**

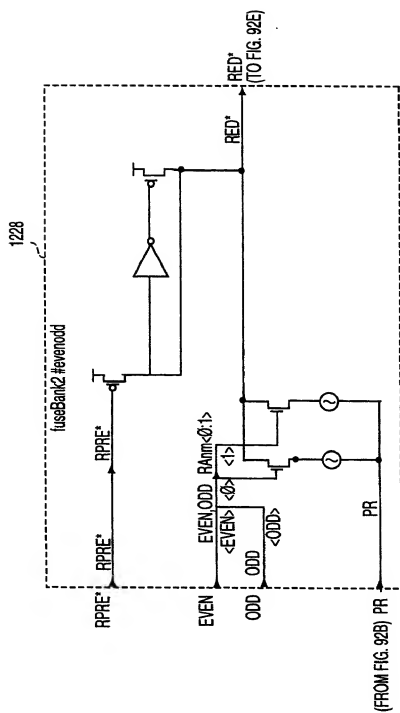
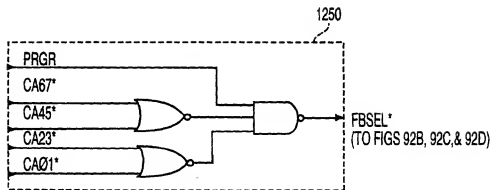


FIG. 92D

**FIG. 93A**

1252

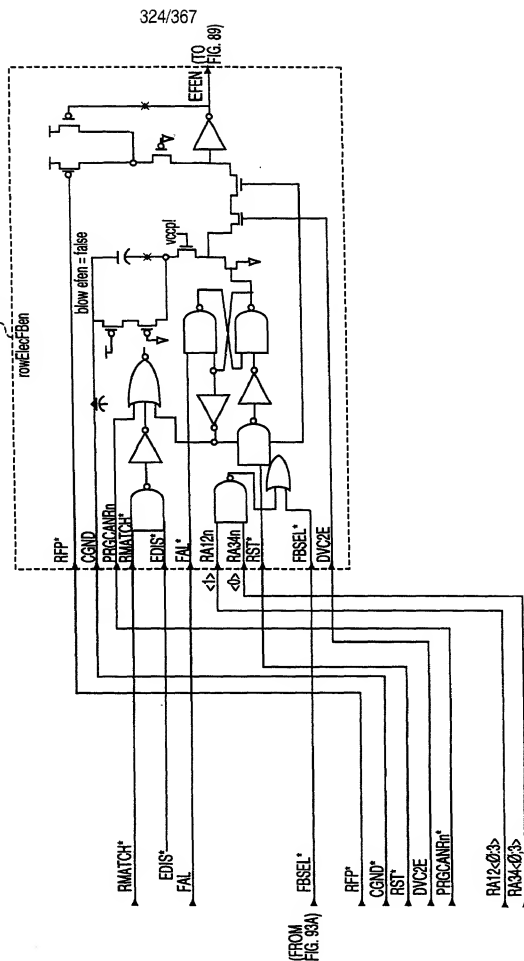


FIG. 93B

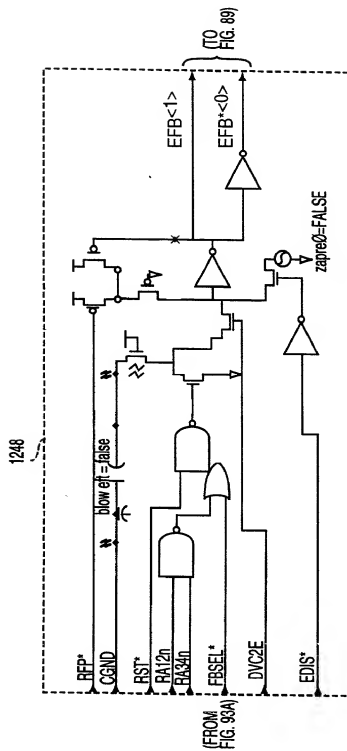


FIG. 93C

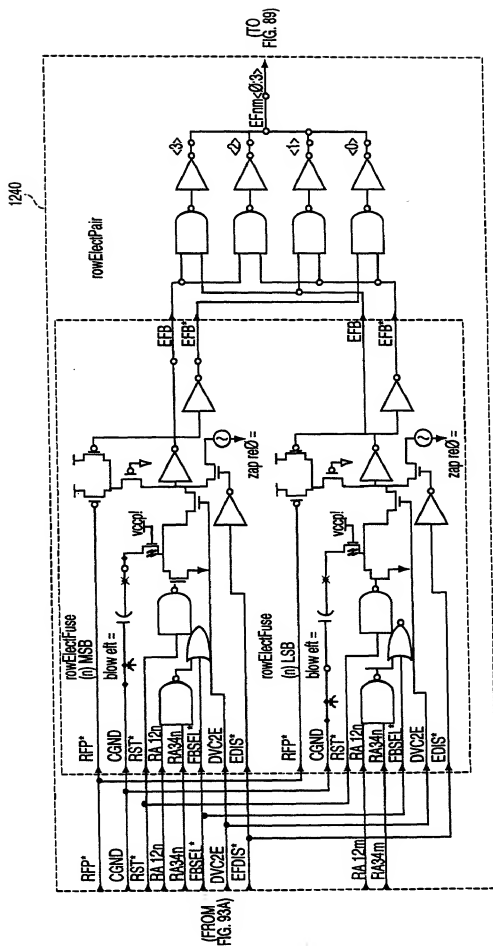
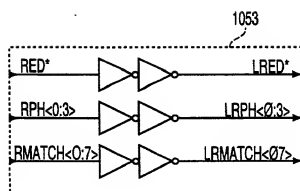


FIG. 93D

**FIG. 94**

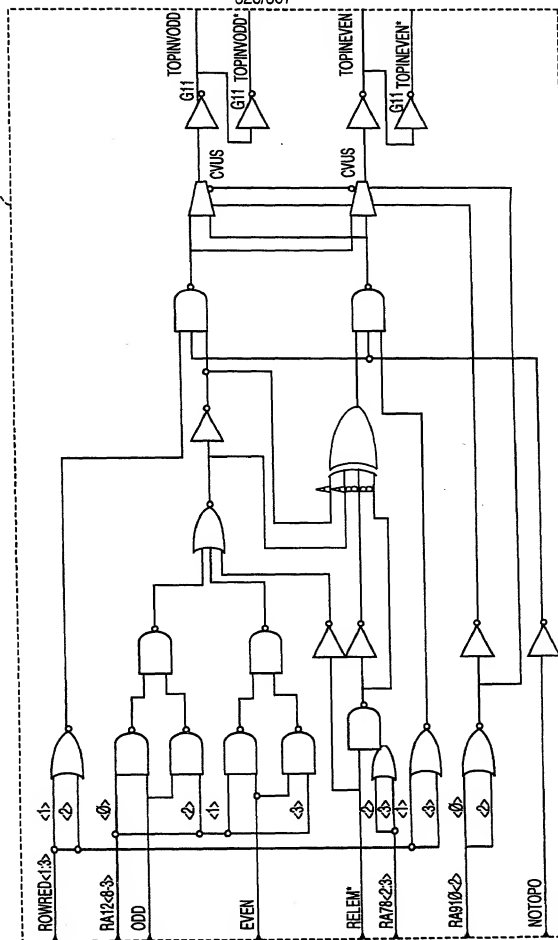


FIG. 95

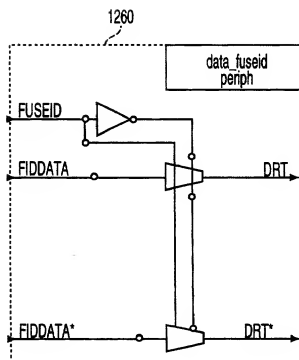
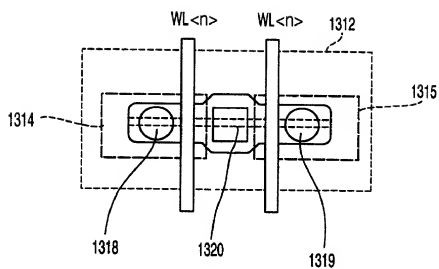
**FIG. 96**



FIG. 97-1 | FIG. 97-2

FIG. 97-1

**FIG. 98**

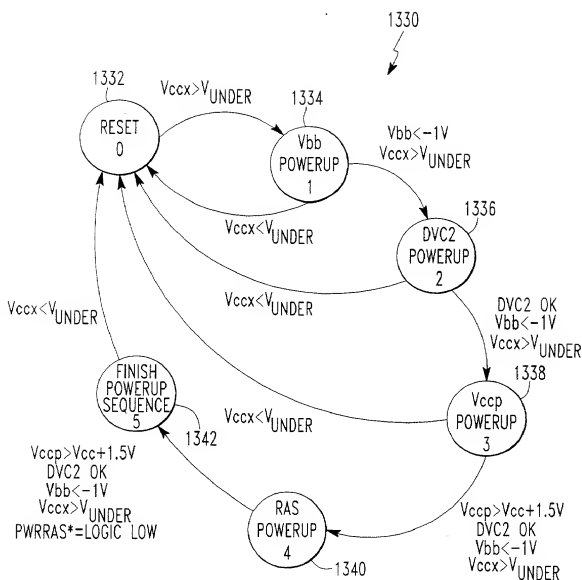


FIG. 99

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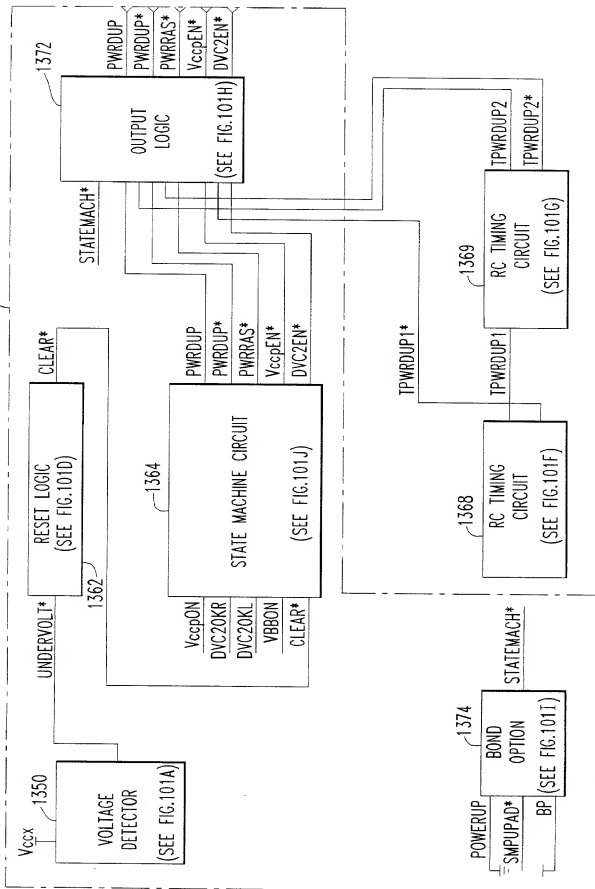


FIG. 100

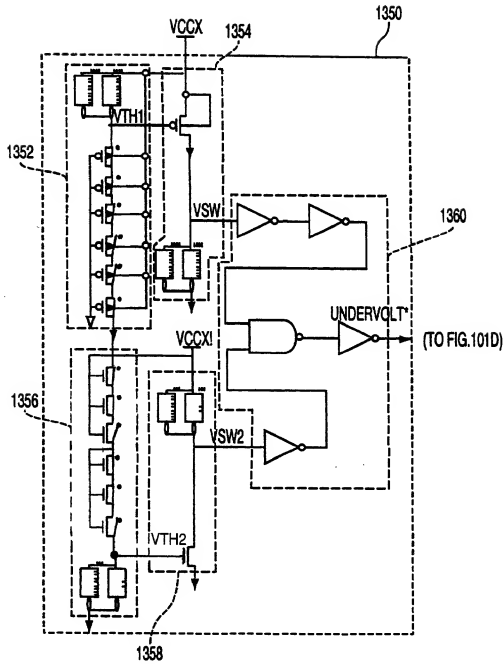
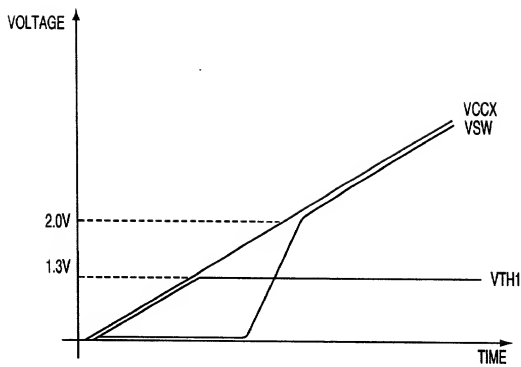
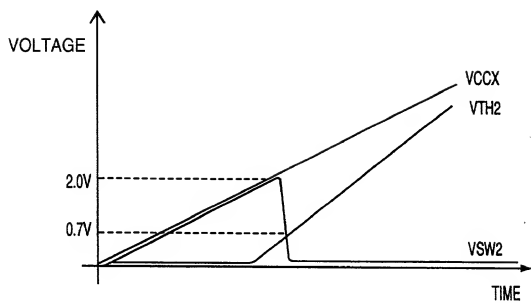


FIG. 101A

**FIG. 101B**

**FIG. 101C**

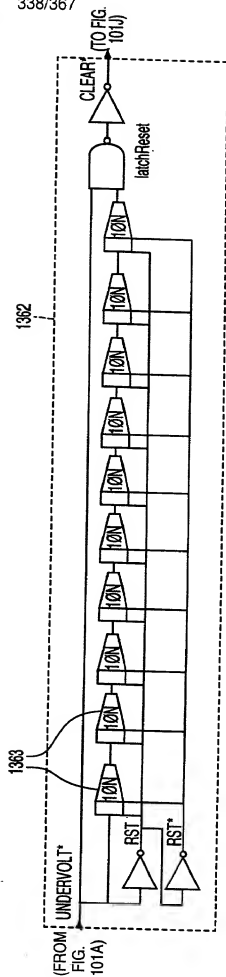


FIG. 101D

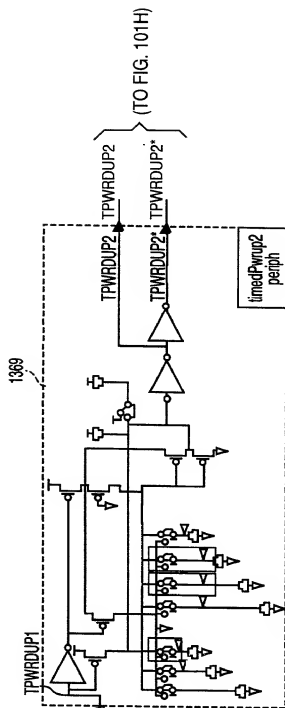


FIG. 101G

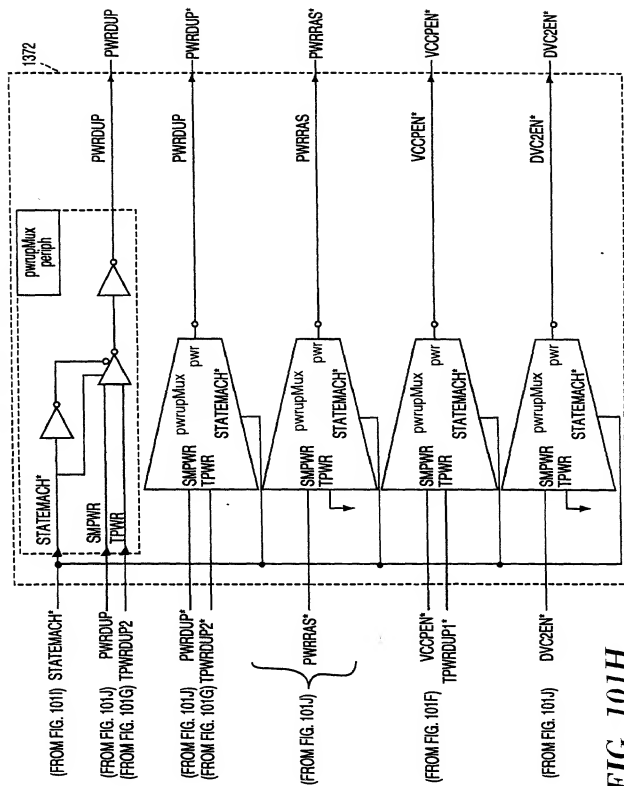


FIG. 101H

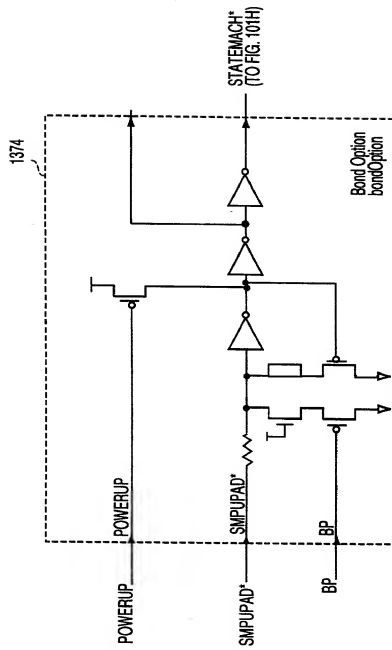


FIG. 101H

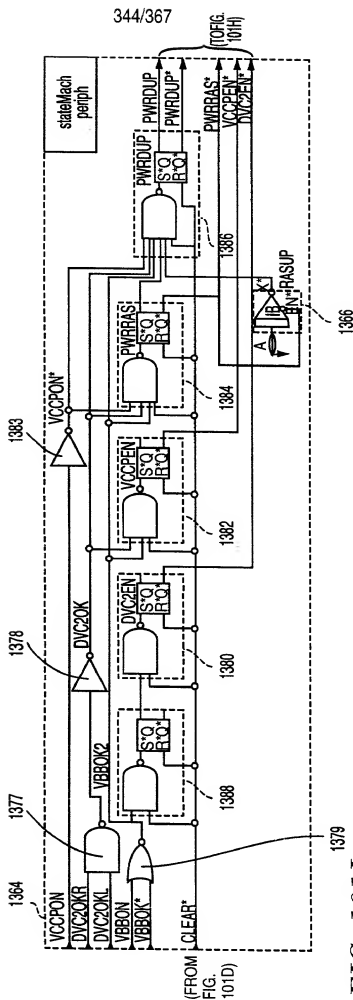
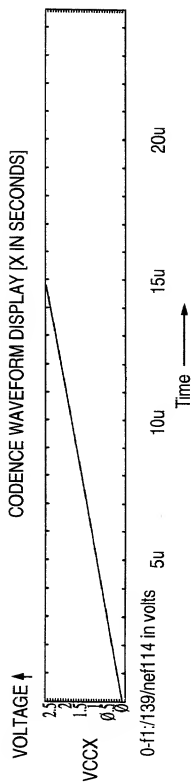
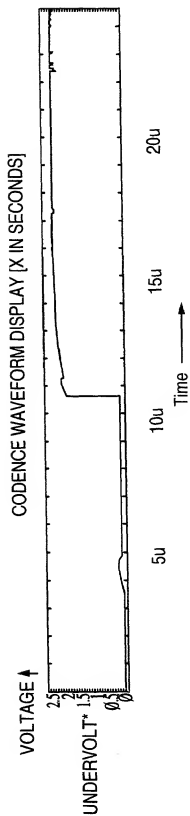


FIG. 101J



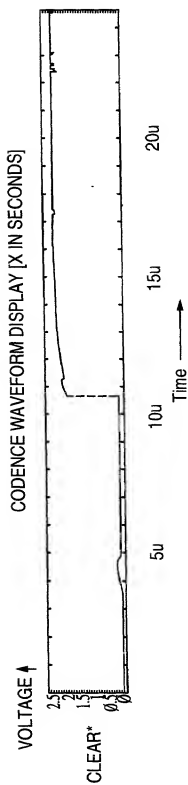
NOTE THAT PWRRAS* WAITED FOR DVC20KR

FIG. 102A



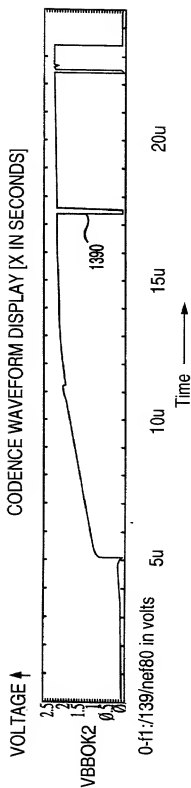
NOTE THAT PWRRAS* WAITED FOR DVC20KR

FIG. 102B



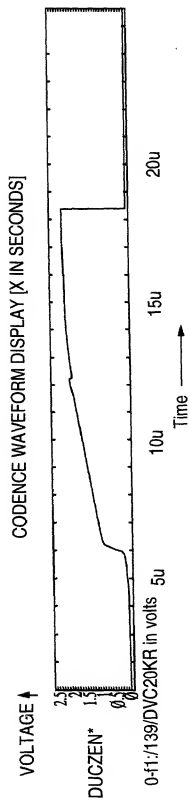
NOTE THAT PWRRAS* WAITED FOR DVC20KR

FIG. 102C



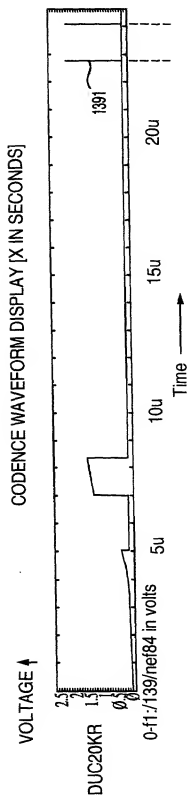
NOTE THAT PWRRAS* WAITED FOR DVC20KR

FIG. 102D



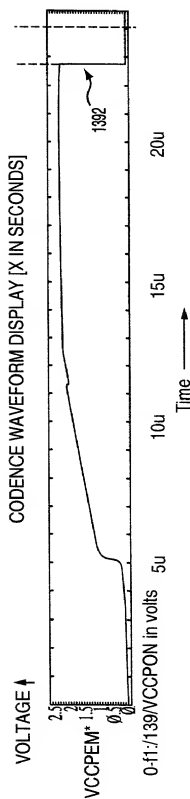
NOTE THAT PWRBAS* WAITED FOR DVC20KR

FIG. 102E



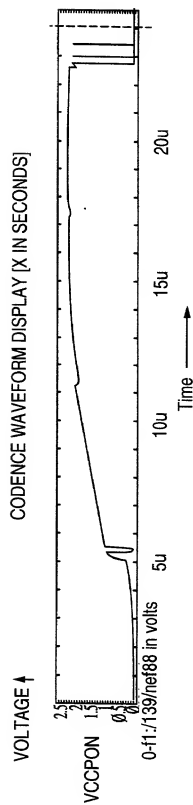
NOTE THAT PWRRAS* WAITED FOR DVC20KR

FIG. 102F



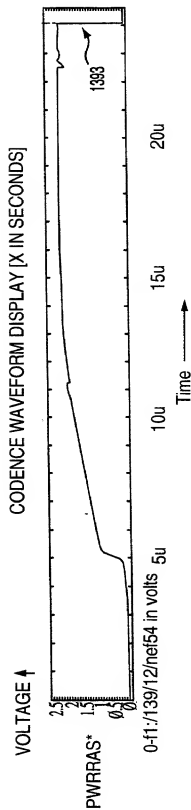
NOTE THAT PWRRAS* WAITED FOR DVC20KR

FIG. 102G



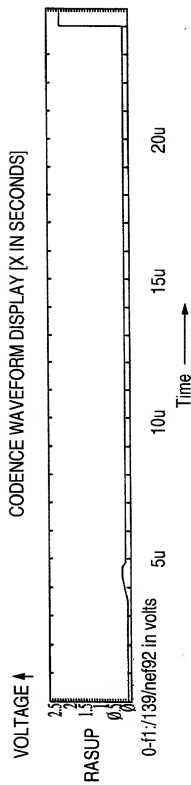
NOTE THAT PWRRAS* WAITED FOR DVC20KR

FIG. 102H



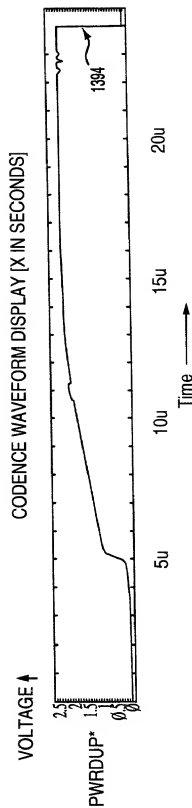
NOTE THAT PWRRAS* WAITED FOR DVC20KR

FIG. 1021



NOTE THAT PWRRAS* WAITED FOR DVC20KR

FIG. 102J



NOTE THAT PWRRAS* WAITED FOR DVC20KR

FIG. 102K

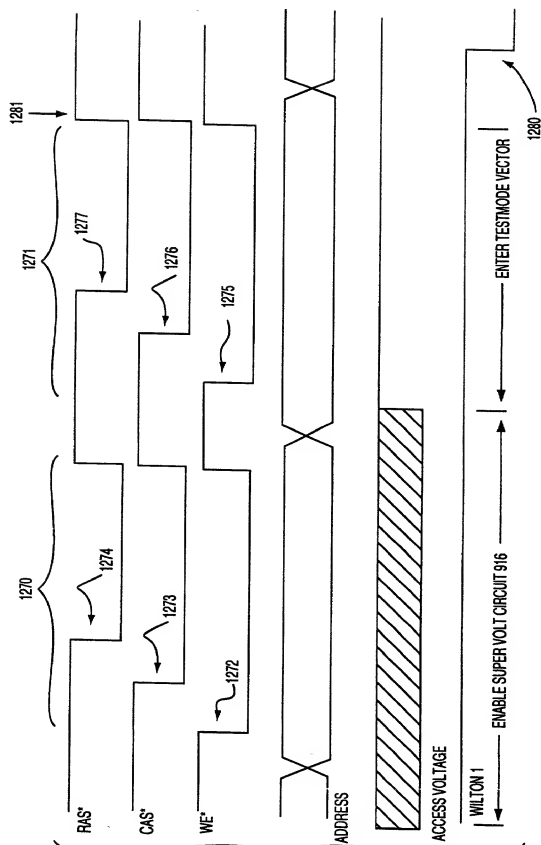
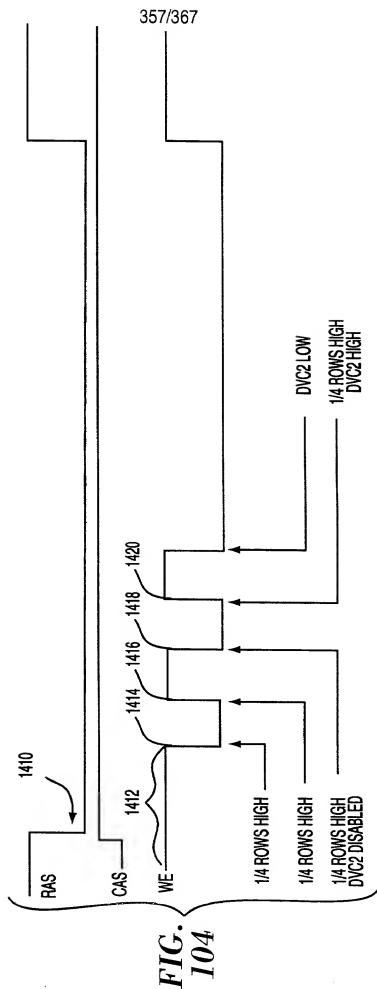
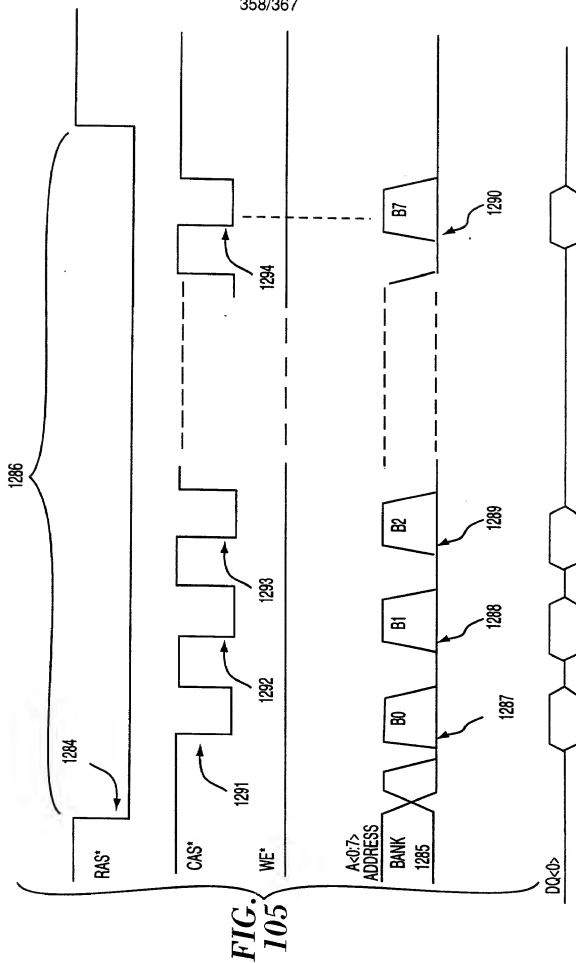
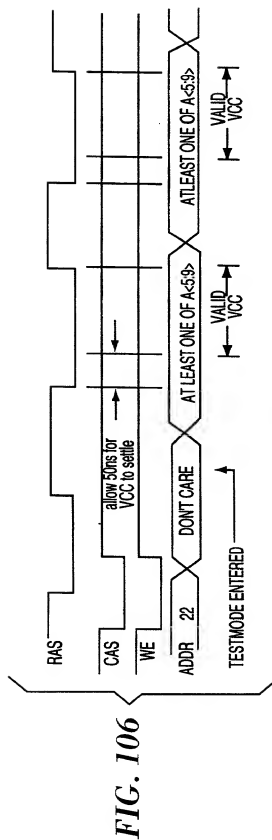


FIG.
103







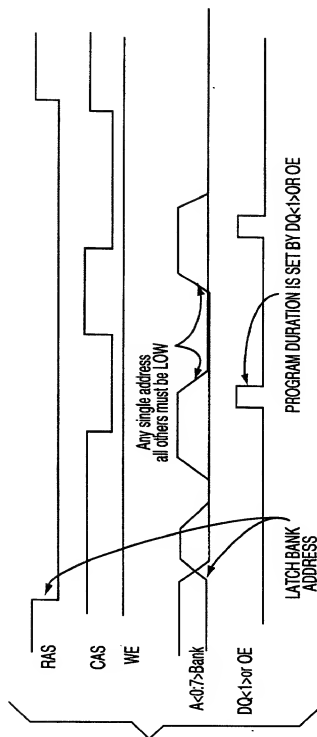


FIG. 107

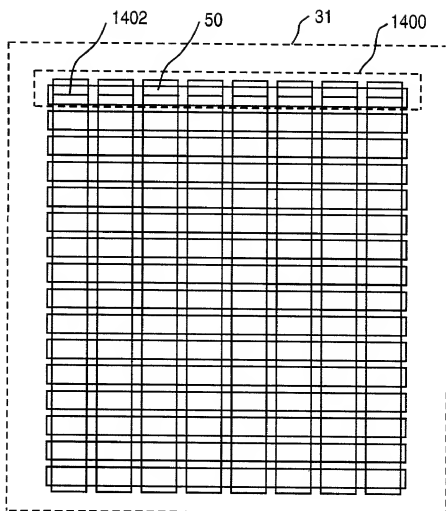
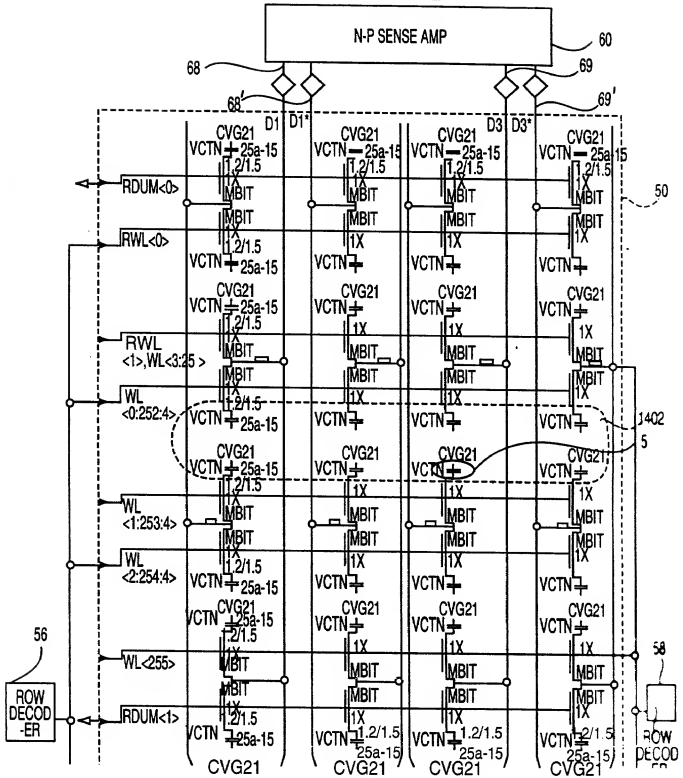
**FIG. 108**

FIG. 109-2



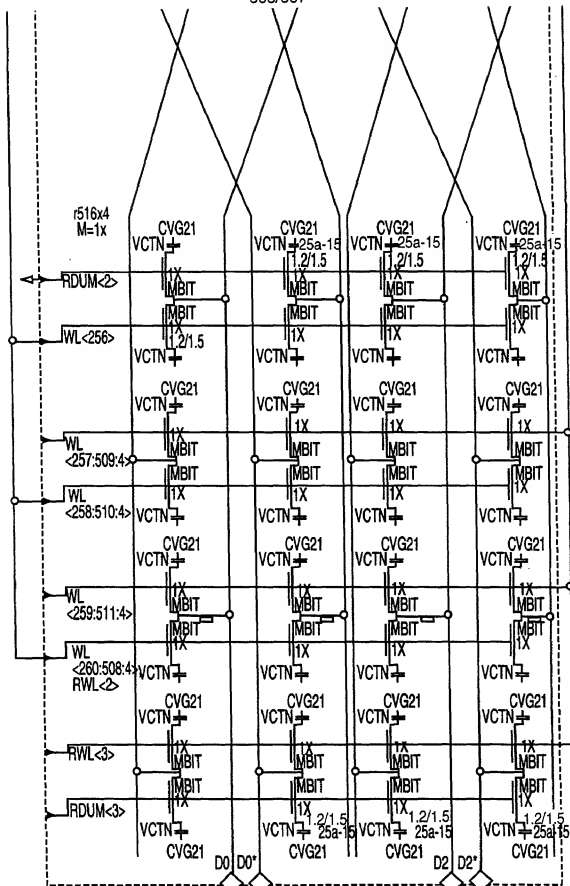


FIG. 109-1

FIG. 109-2

FIG. 109-2

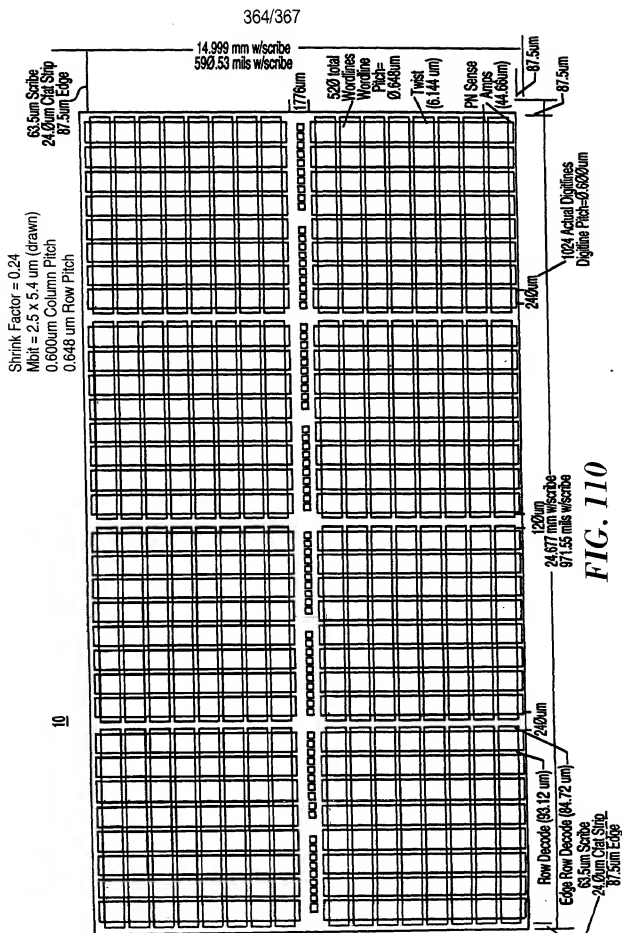
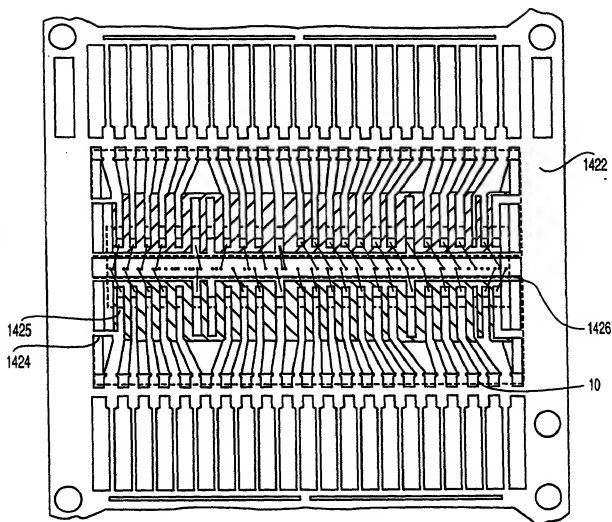


FIG. 110



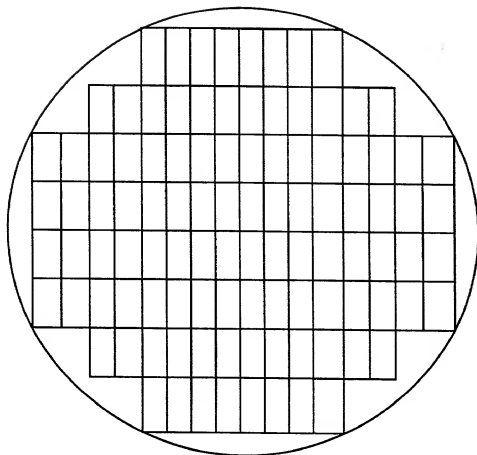


FIG. 112

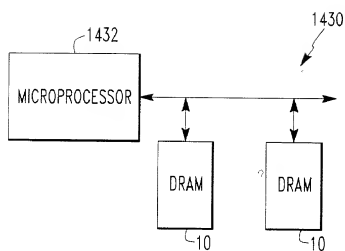


FIG. 113

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